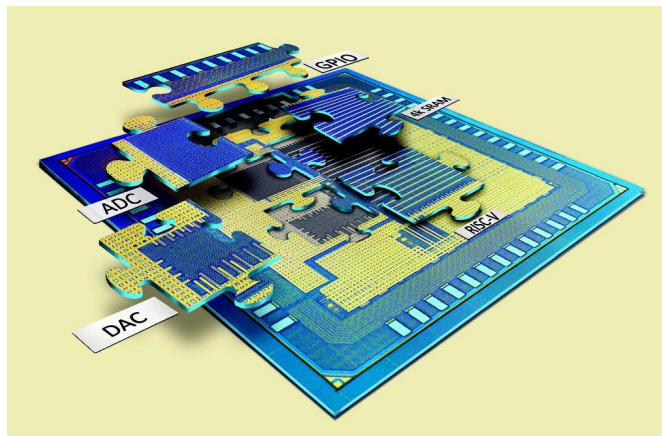
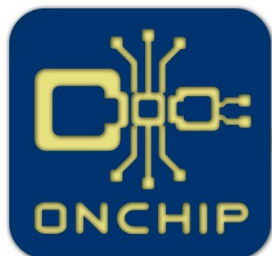


RISC-V Community needs Peripheral Cores



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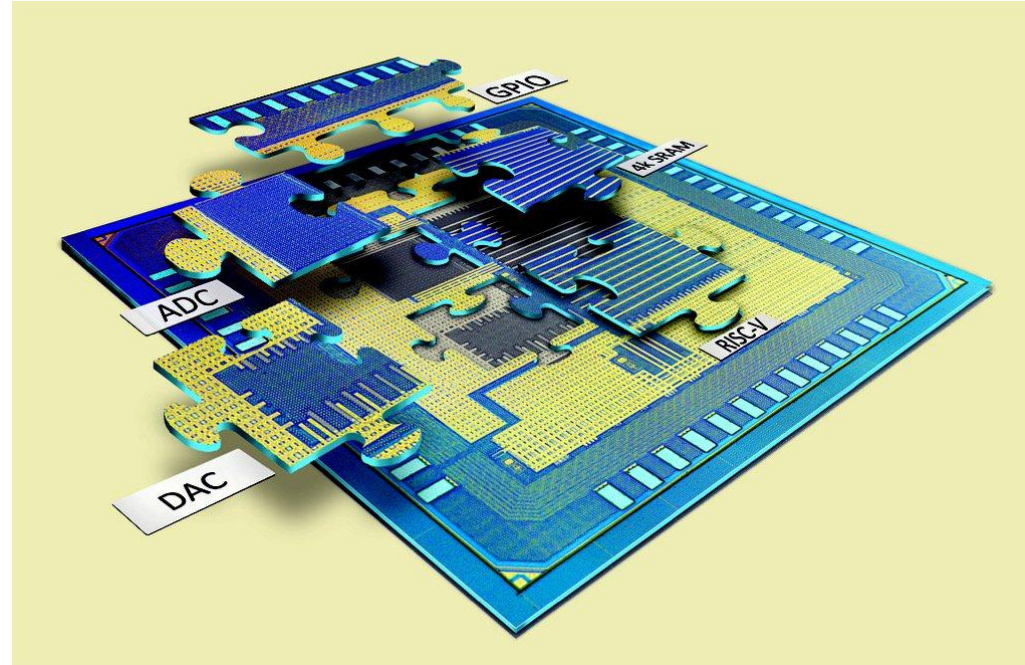


@onchipUIS



Good to have an Open ISA. What about Peripheral?

- IP vendors have IP based on previous customer. **Hard to get** a glue-and-play that works for your SoC. → \$\$\$
- There are some std, such as PHYs: USB, LPDDR, PCIe, AMBA
BUT
no for clocking circuitry, biasing, GPIO
For instance a simple Power-on-Reset can hit your pocket, just because!
- Buses IP are out there but expensive.
Why: Similar to compilers decades ago

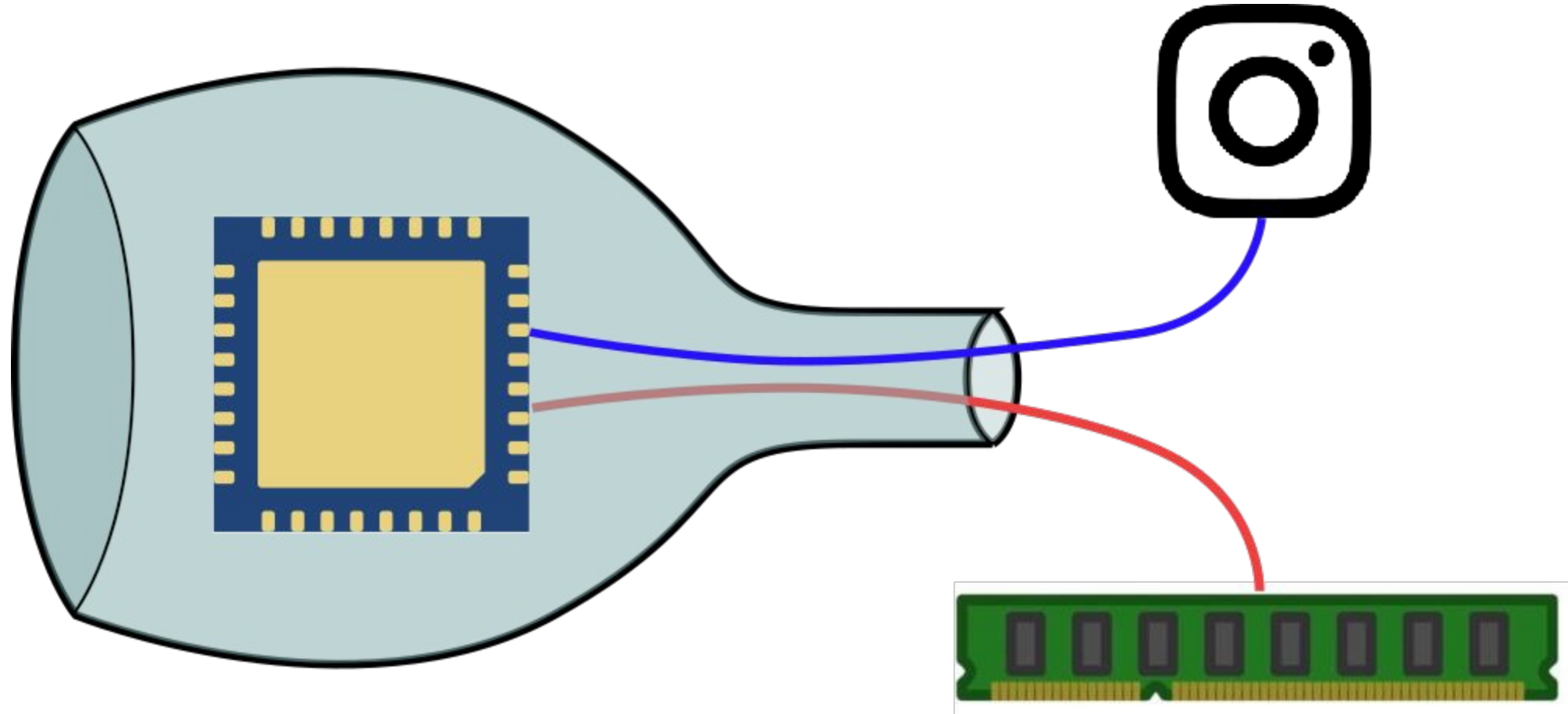


Can we do better?
We might

Agenda

- 1. Why we need more open-std silicon-HW?**
- 2. IC Community can build up peripheral. Our case.**
- 3. Suggestion and take away.**

Case 1: Receiving/Sending Data Bottleneck

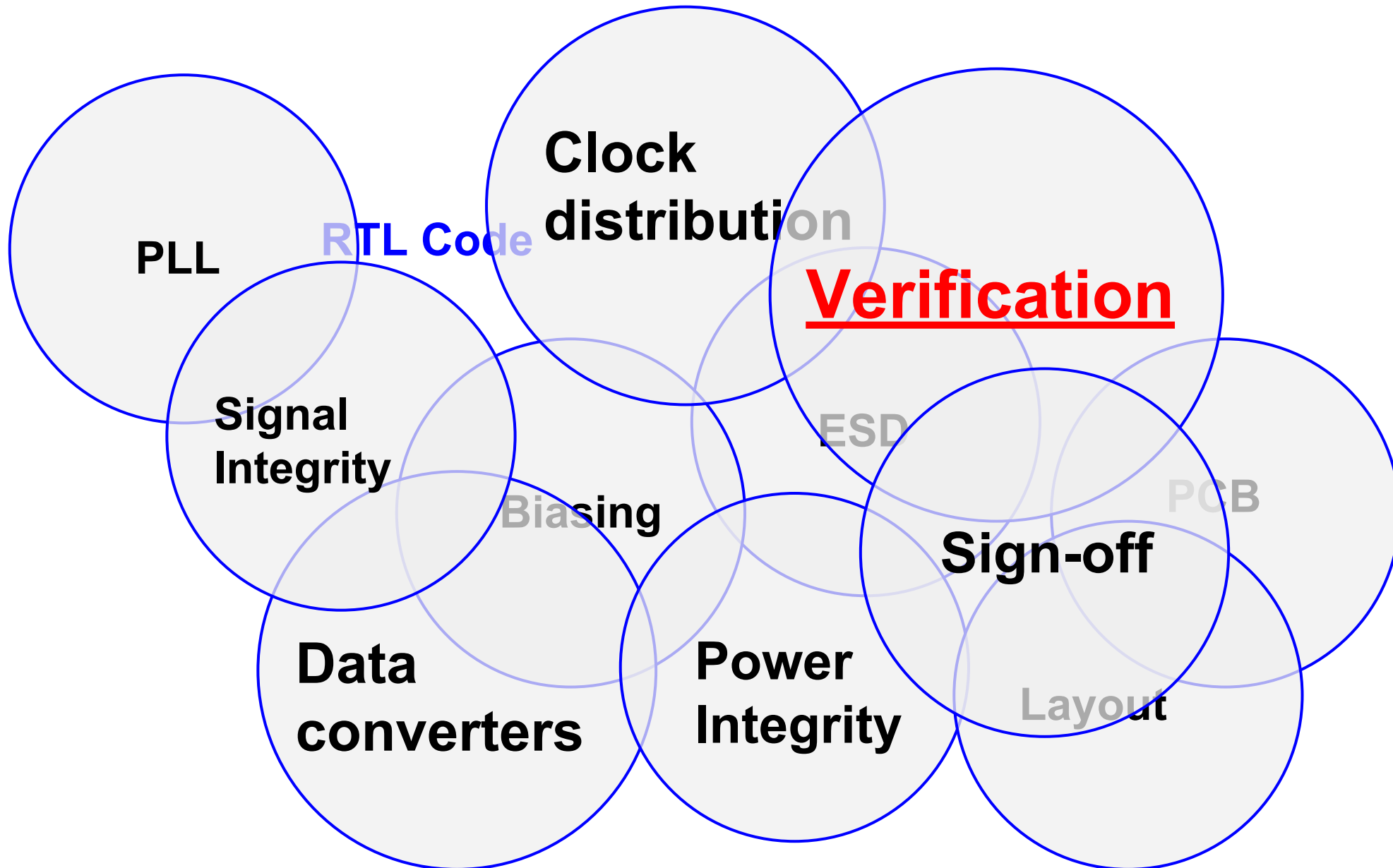


Suggestion: RISC-V Recommends

Open-IP Bus	RISC-V core used	Provider	Repository	Functional Model	Silicon proven
SPI	Rocket/Open-V/ Epihany-V	Adapteva	github.com/adapteva	✓	✓
I2C	Open-V/Pulp	Onchip/Pulp	github.com/onchipUIS	✓	✓
AXI-4.0					
APB-4.0					
AHB-2.0					
USB 2.0 PHY					
USB 3.1 PHY					
RapidIO					
LPDDR3					

- Compliance test suite - Functional model → UVM

Lot of circuits, lot of skills



Take away

- **Don't get your SoC-idea stuck just because you don't have regular IP.**
- **We need more standard Peripherals.**
- **Don't reinvent the wheel. We need to join efforts.**

Support us!

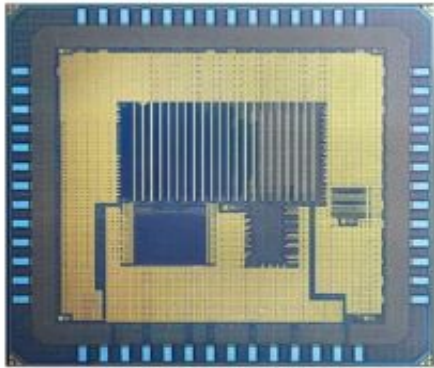
CROWD SUPPLY

Creators → OnChip

Open-V

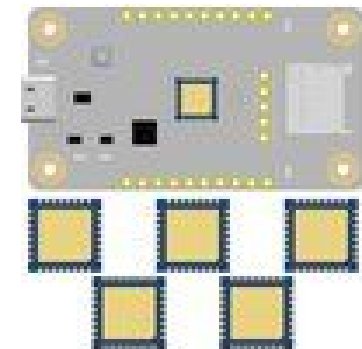
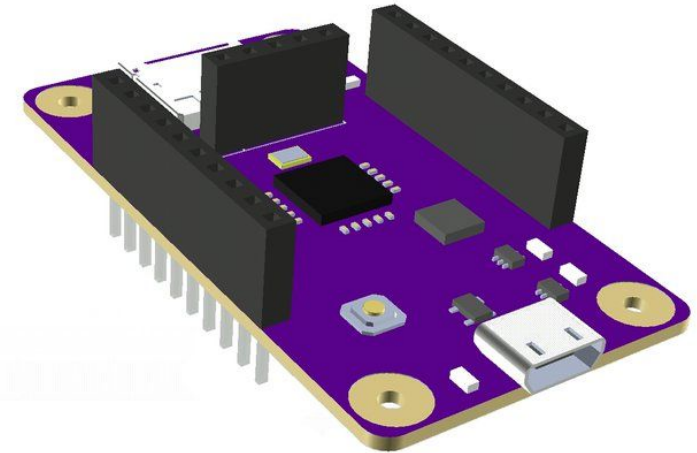
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01:21

\$20,013 raised
of \$480,000 goal



<https://www.crowdsupply.com/onchip/open-v>