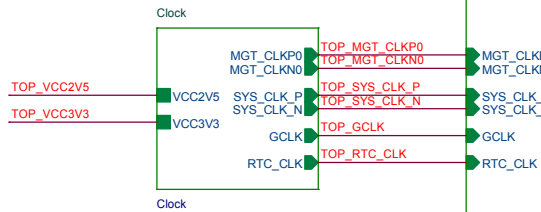
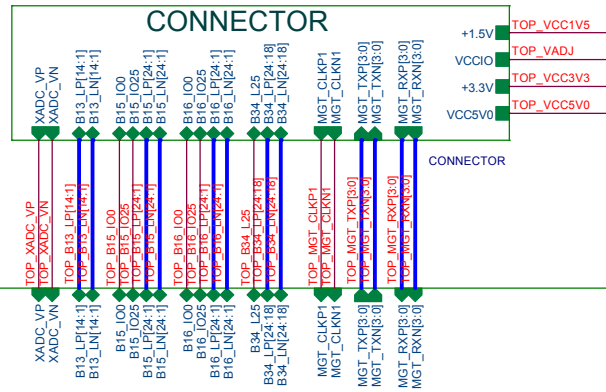
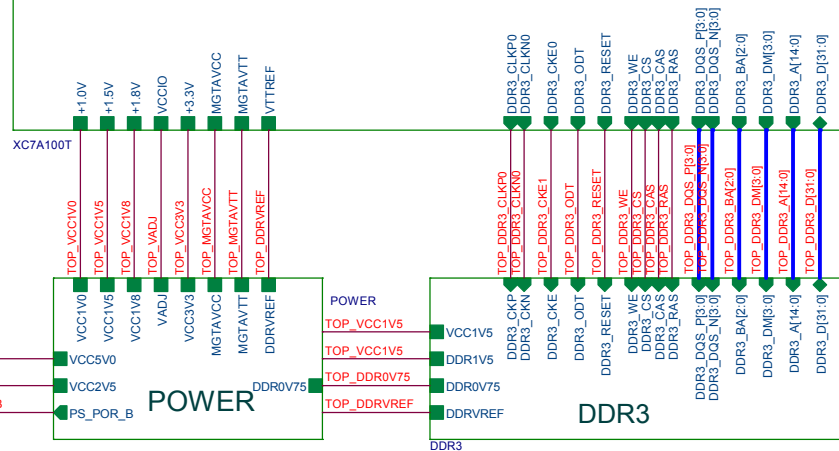
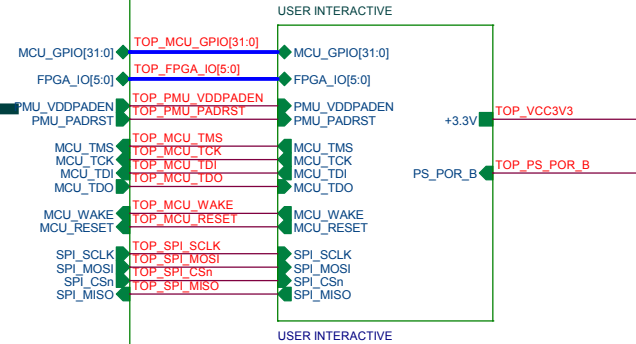


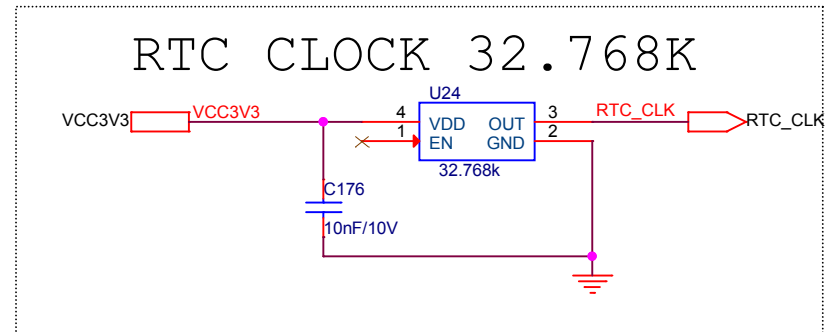
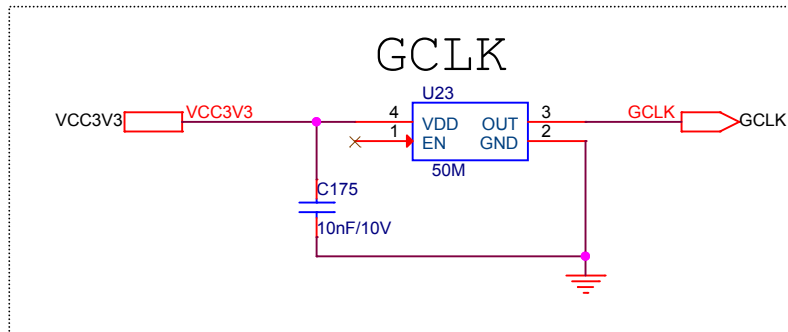
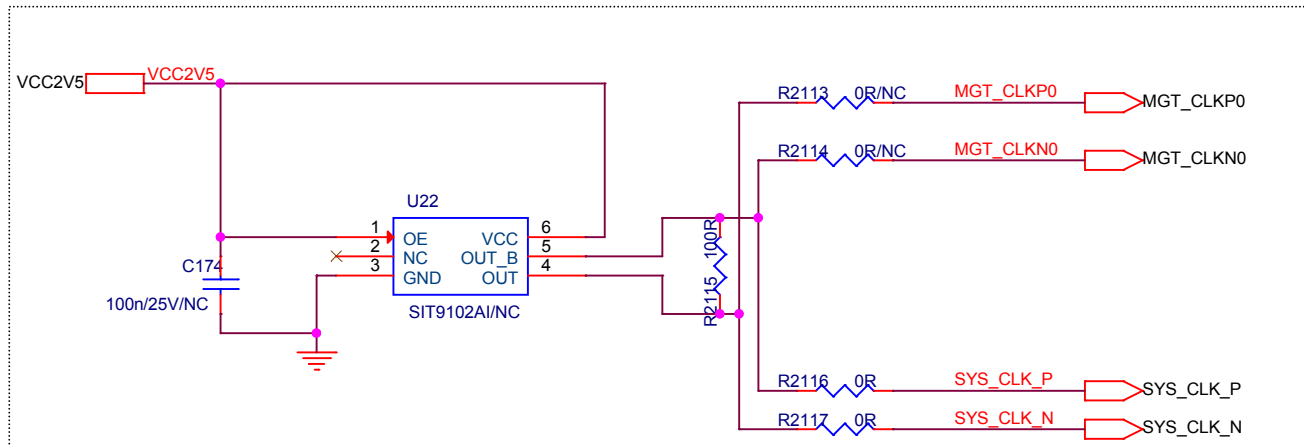
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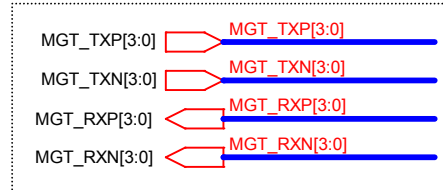
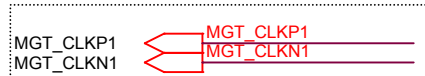
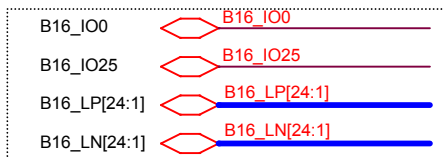
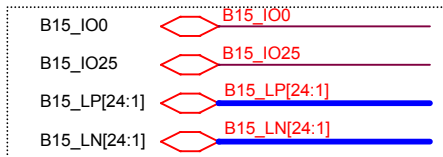
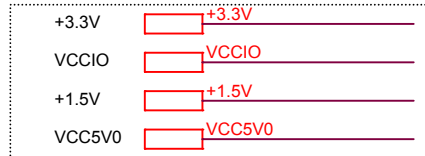
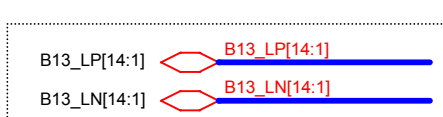
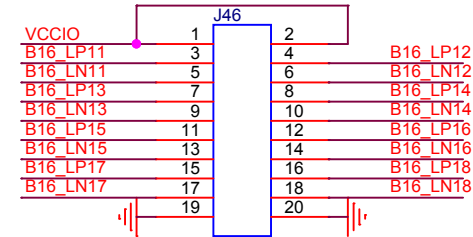
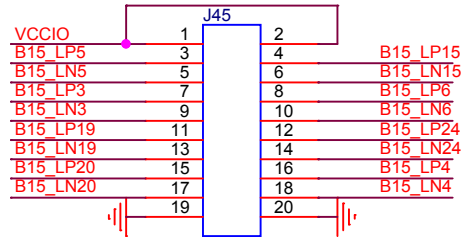
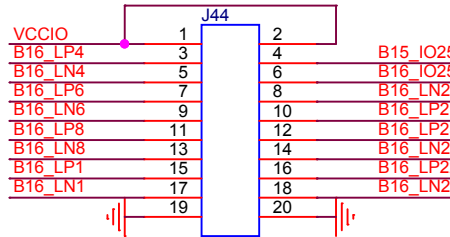
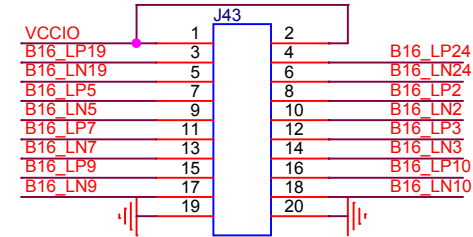
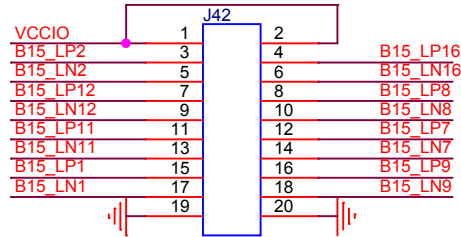
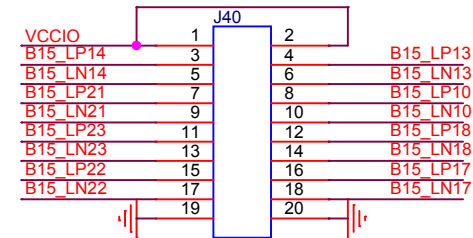
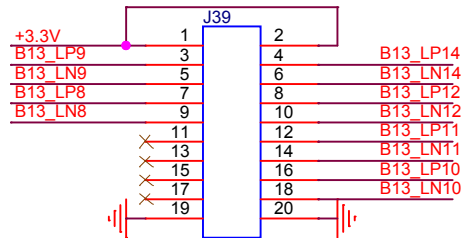
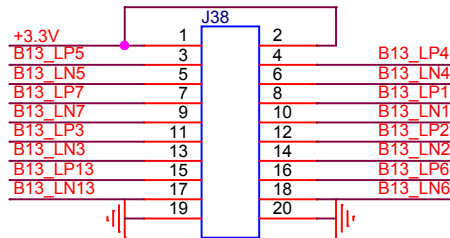
XC7A100T



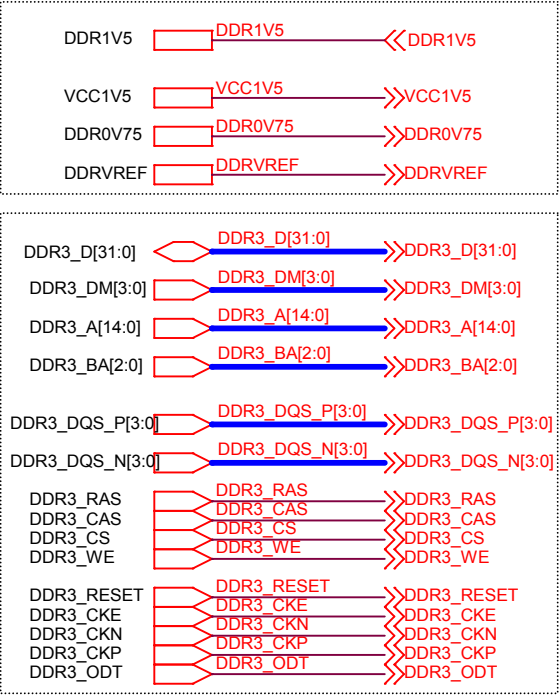
CLOCK



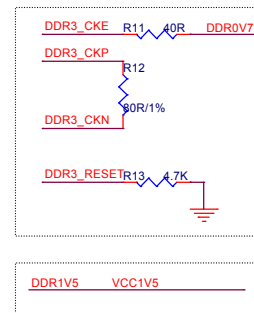
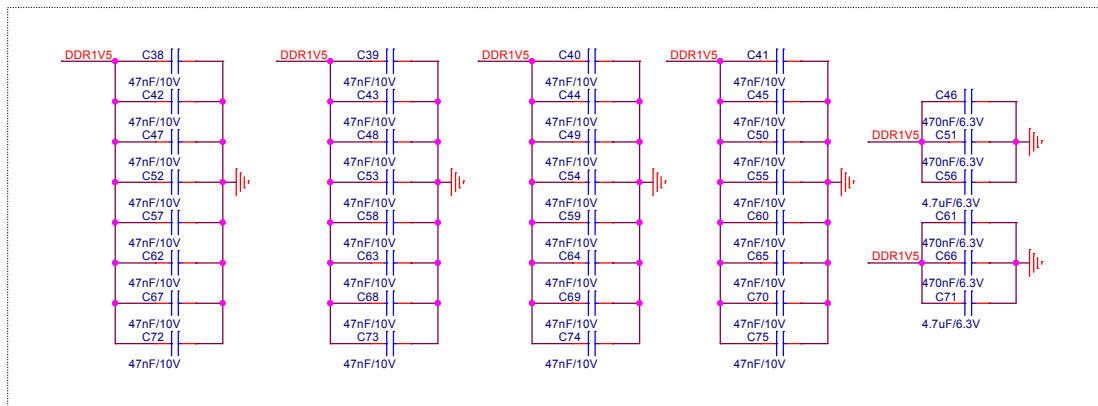
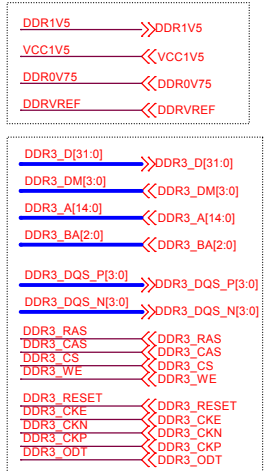
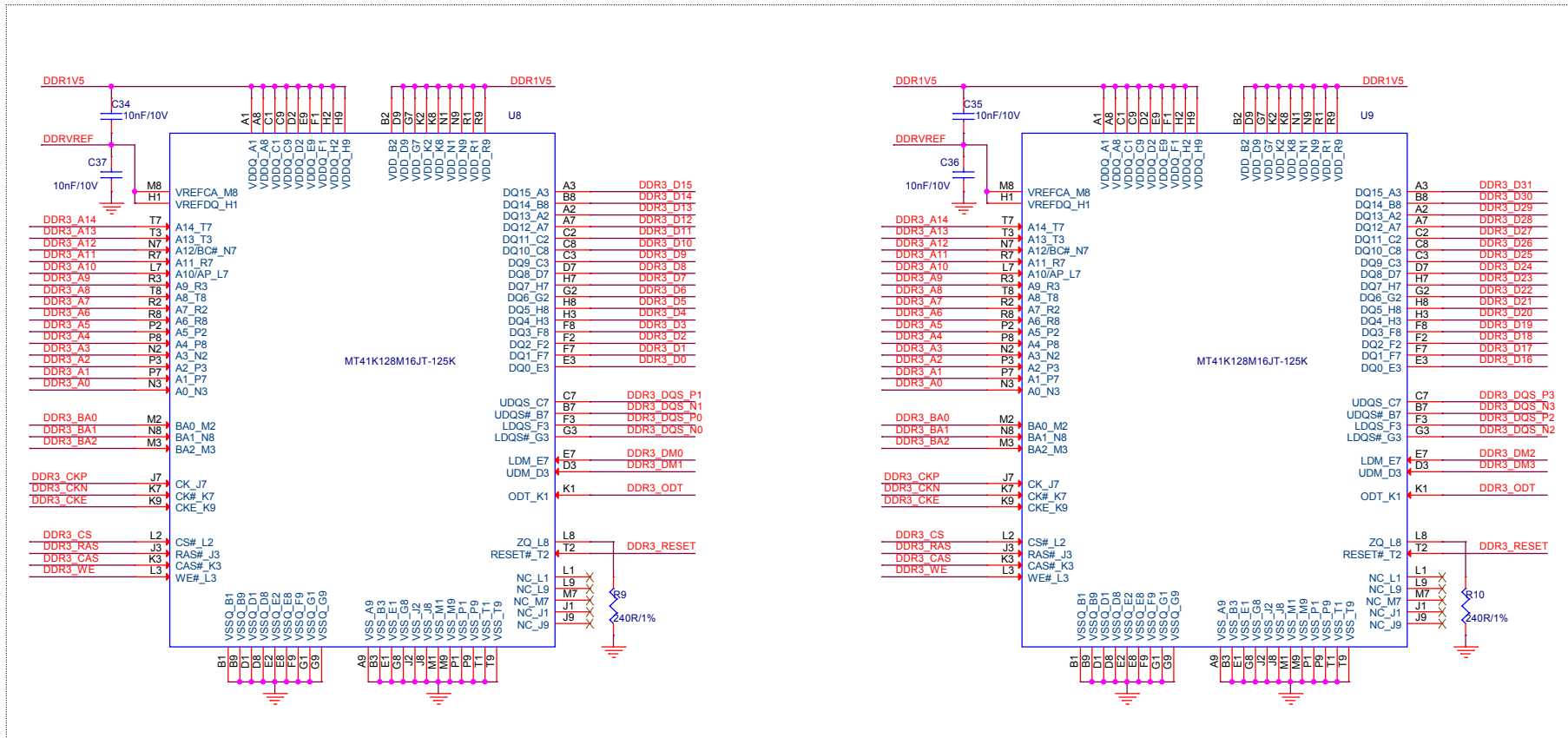
CONNECTOR



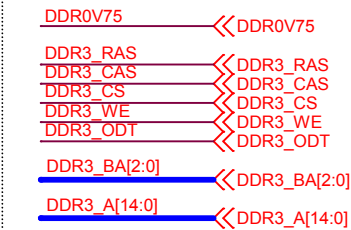
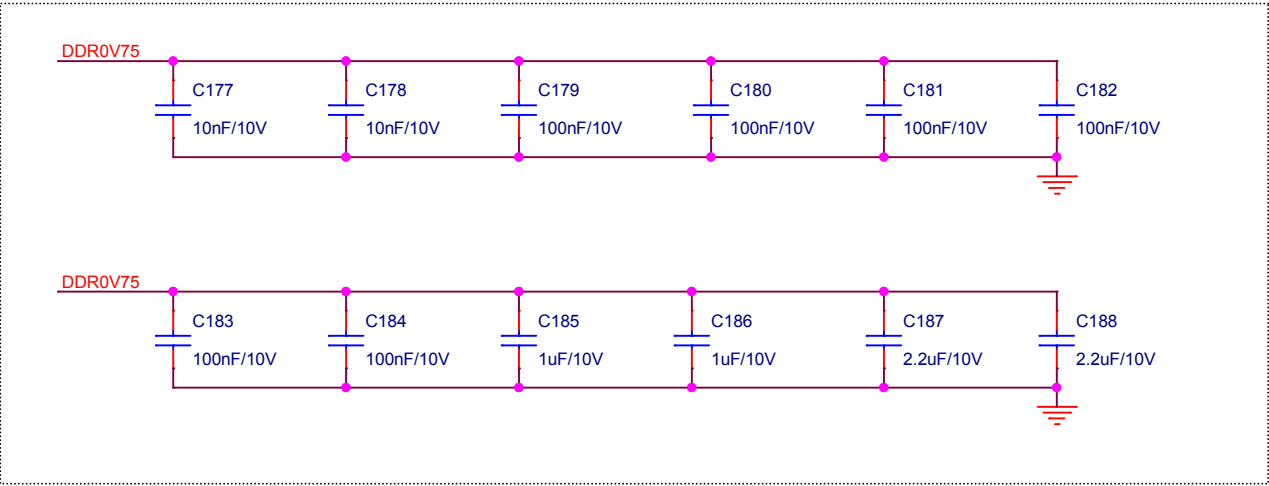
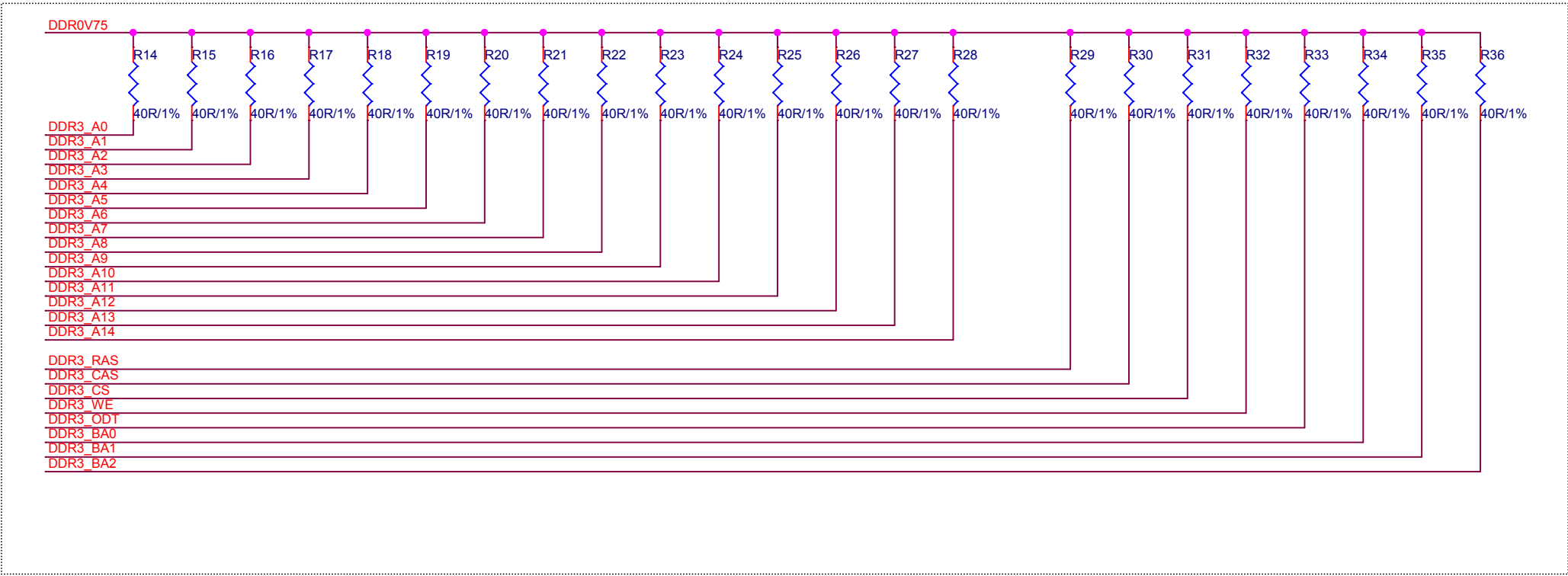
DDR3 TO TOP PORT



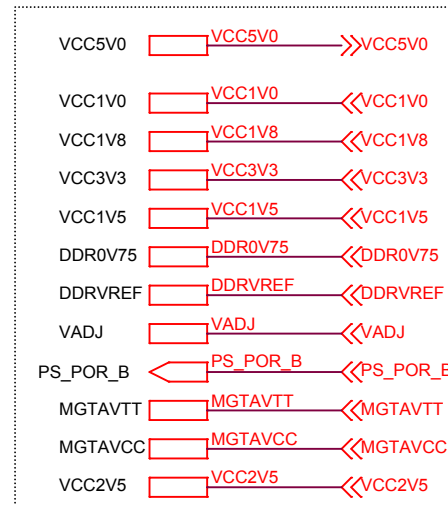
DDR3 SDRAM



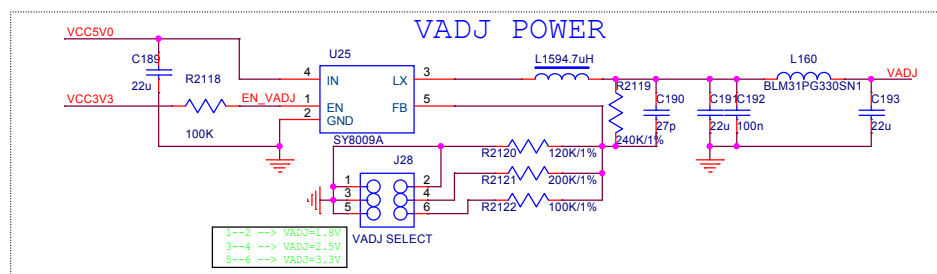
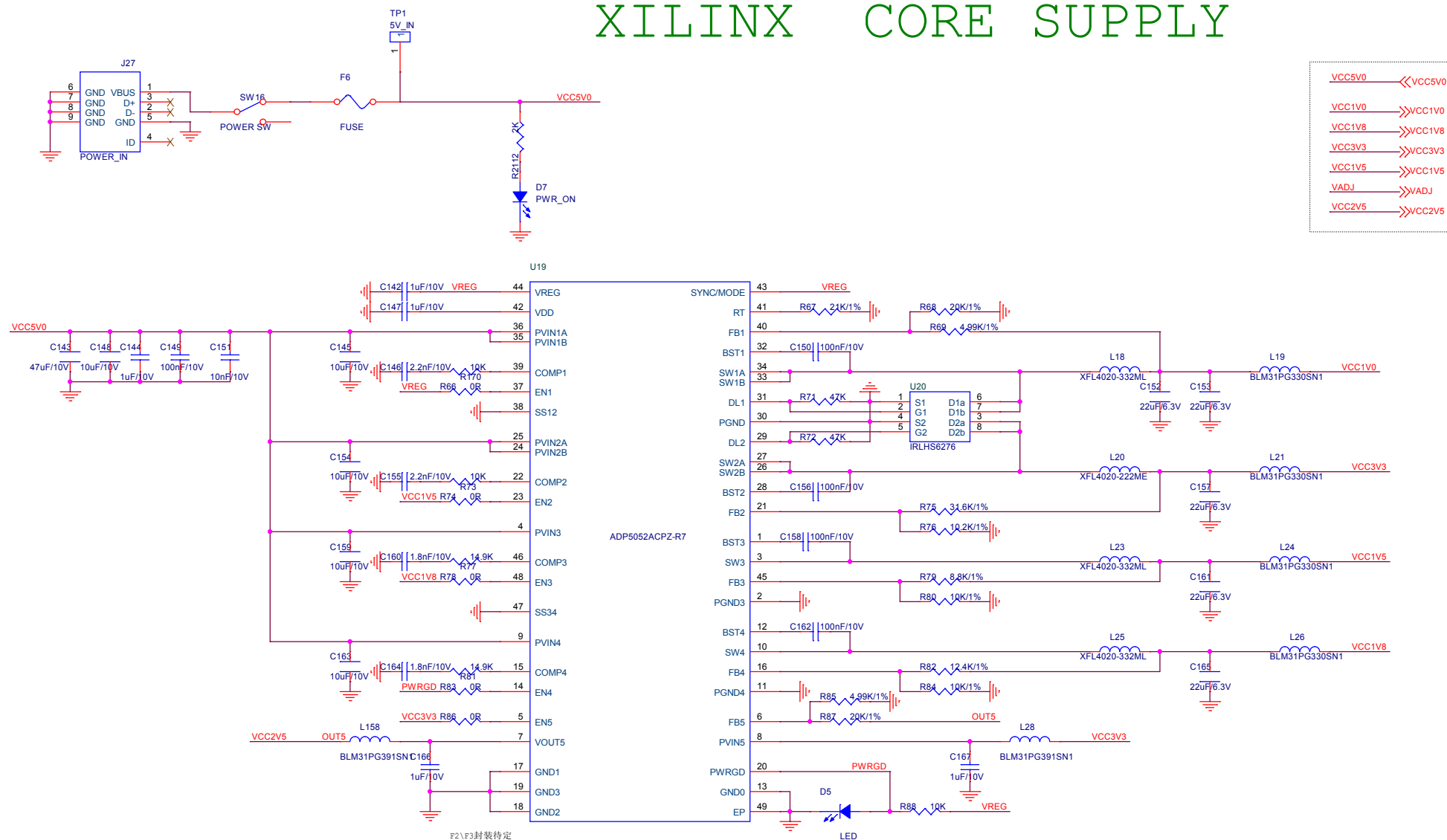
DDR3 TERMINATION



POWER TO TOP

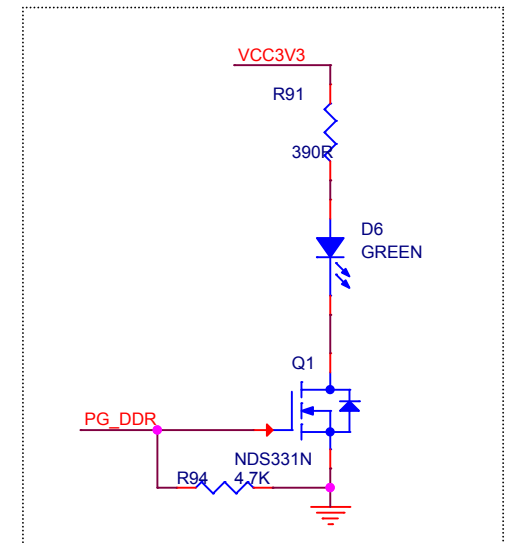
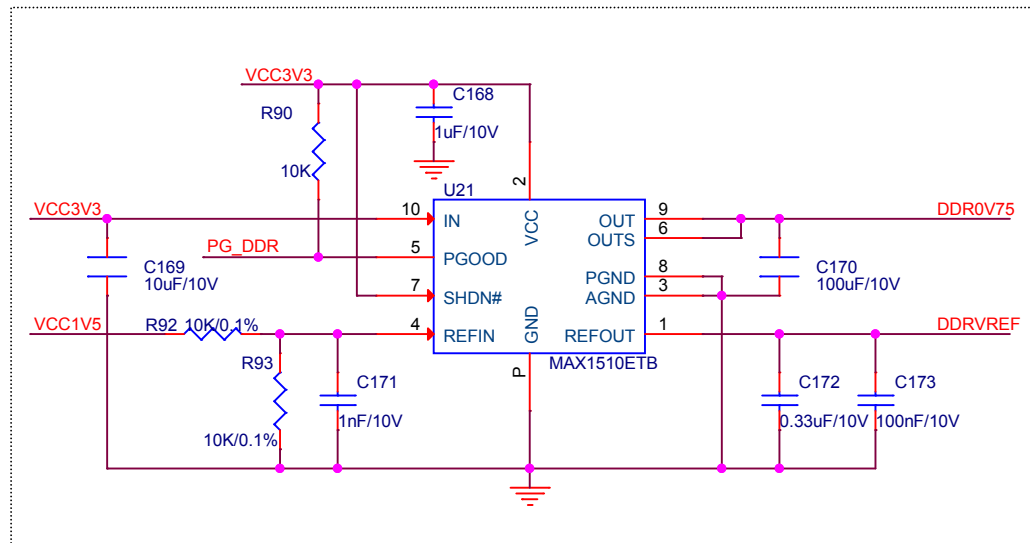
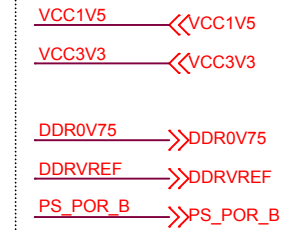


XILINX CORE SUPPLY



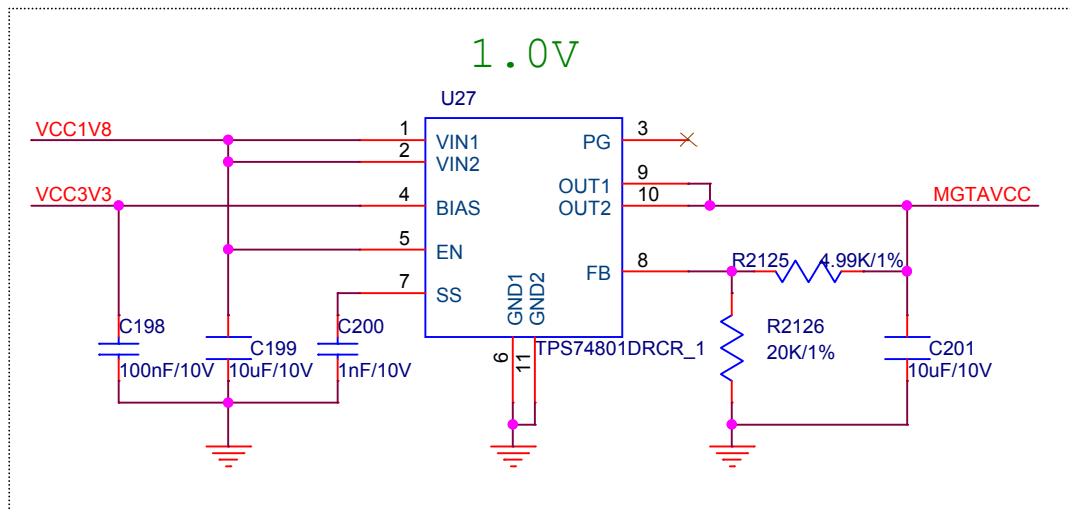
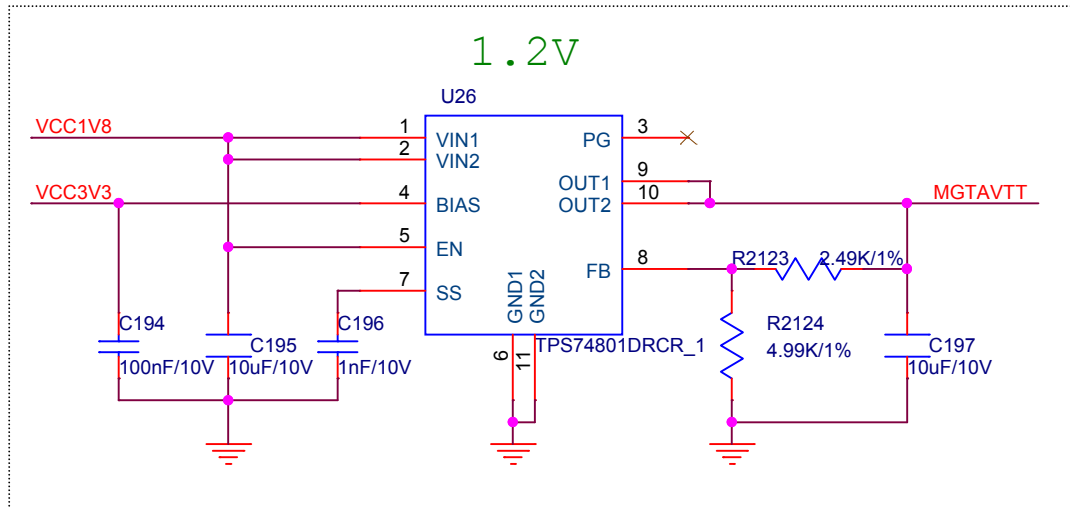
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DDR3 SUPPLY



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MGT POWER



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Page Name MGT SUPPLY

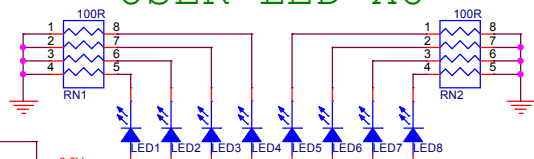
Rev
V0.1

Date: Tuesday, October 30, 2018

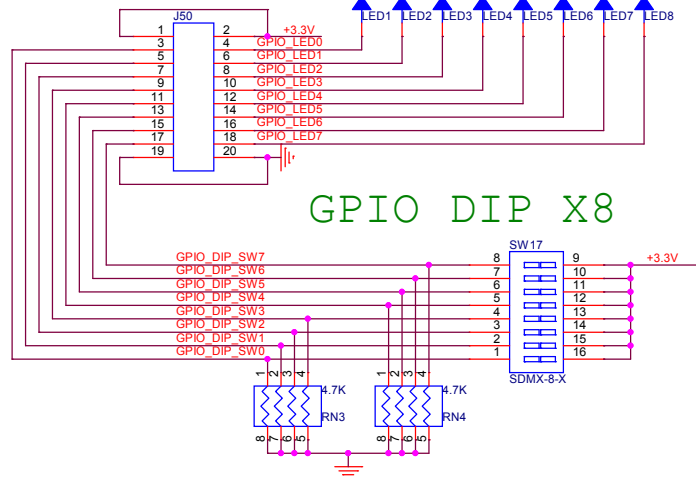
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USER INTERACTIVE

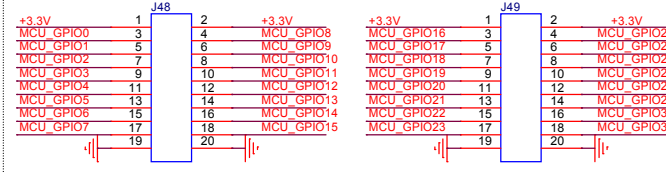
USER LED X8



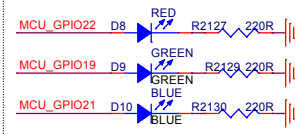
GPIO DIP X8



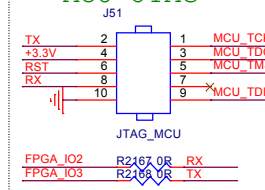
GPIO JACK



USER LED



MCU JTAG



+3.3V <--> +3.3V <--> +3.3V

MCU_GPIO[31:0] <--> MCU_GPIO[31:0]

FPGA_IO[5:0] <--> FPGA_IO[5:0]

MCU_WAKE <--> MCU_WAKE
MCU_RESET <--> MCU_RESET

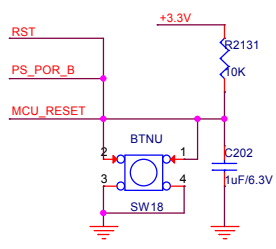
MCU_TDI <--> MCU_TDI
MCU_TDO <--> MCU_TDO
MCU_TMS <--> MCU_TMS
MCU_TCK <--> MCU_TCK

PS_POR_B <--> PS_POR_B

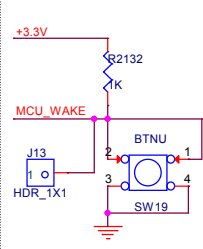
PMU_VDDPADEN <--> PMU_VDDPADEN
PMU_PADDRST <--> PMU_PADDRST

SPI_MISO <--> SPI_MISO
SPI_MOSI <--> SPI_MOSI
SPI_SCLK <--> SPI_SCLK
SPI_CS_n <--> SPI_CS_n

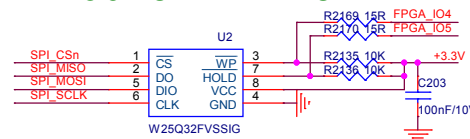
MCU RESET



MCU WAKE



MCU SPI FLASH



XC7A100T PORT TO TOP

+1.0V >>> +1.0V
+1.5V >>> +1.5V
+1.8V >>> +1.8V
+3.3V >>> +3.3V
VCCIO >>> VCCIO
MGTA VCC >>> MGTA VCC
MGTA VTT >>> MGTA VTT
VTTREF >>> VTTREF

XADC_VP >>> XADC_VP
XADC_VN >>> XADC_VN

MCU_GPIO[31:0] >>> MCU_GPIO[31:0]
FPGA_IO[5:0] >>> FPGA_IO[5:0]
MCU_WAKE >>> MCU_WAKE
MCU_RESET >>> MCU_RESET

MCU_TDI >>> MCU_TDI
MCU_TDO >>> MCU_TDO
MCU_TMS >>> MCU_TMS
MCU_TCK >>> MCU_TCK

MGT_TXP[3:0] >>> MGT_TXP[3:0]
MGT_TXN[3:0] >>> MGT_TXN[3:0]
MGT_RXP[3:0] >>> MGT_RXP[3:0]
MGT_RXN[3:0] >>> MGT_RXN[3:0]

MGT_CLKP0 >>> MGT_CLKP0
MGT_CLKN0 >>> MGT_CLKN0
MGT_CLKP1 >>> MGT_CLKP1
MGT_CLKN1 >>> MGT_CLKN1

B34_LP[24:18] >>> B34_LP[24:18]
B34_LN[24:18] >>> B34_LN[24:18]
B34_L25 >>> B34_L25

SYS_CLK_P >>> SYS_CLK_P
SYS_CLK_N >>> SYS_CLK_N

DDR3_A[14:0] >>> DDR3_A[14:0]
DDR3_D[31:0] >>> DDR3_D[31:0]
DDR3_DQS_P[3:0] >>> DDR3_DQS_P[3:0]
DDR3_DQS_N[3:0] >>> DDR3_DQS_N[3:0]
DDR3_DM[3:0] >>> DDR3_DM[3:0]
DDR3_BA[2:0] >>> DDR3_BA[2:0]
DDR3_CLKP0 >>> DDR3_CLKP0
DDR3_CLKN0 >>> DDR3_CLKN0
DDR3_WE >>> DDR3_WE
DDR3_RAS >>> DDR3_RAS
DDR3_CAS >>> DDR3_CAS
DDR3_CKE0 >>> DDR3_CKE0
DDR3_ODT >>> DDR3_ODT
DDR3_RESET >>> DDR3_RESET
DDR3_CS >>> DDR3_CS

B13_LP[14:1] >>> B13_LP[14:1]
B13_LN[14:1] >>> B13_LN[14:1]

B15_IO0 >>> B15_IO0
B15_IO25 >>> B15_IO25
B15_LP[24:1] >>> B15_LP[24:1]
B15_LN[24:1] >>> B15_LN[24:1]

GCLK >>> GCLK
RTC_CLK >>> RTC_CLK

SPI_MISO >>> SPI_MISO
SPI_MOSI >>> SPI_MOSI
SPI_SCLK >>> SPI_SCLK
SPI_CSn >>> SPI_CSn

PMU_VDDPADEN >>> PMU_VDDPADEN
PMU_PADRST >>> PMU_PADRST

B16_IO0 >>> B16_IO0
B16_IO25 >>> B16_IO25
B16_LP[24:1] >>> B16_LP[24:1]
B16_LN[24:1] >>> B16_LN[24:1]



Title

E203 RISC-V评估板

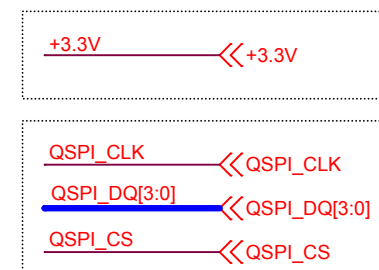
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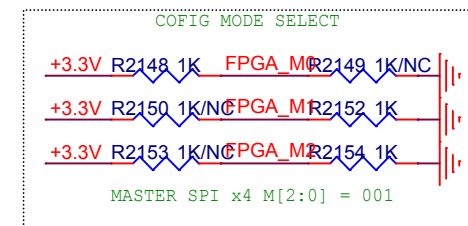
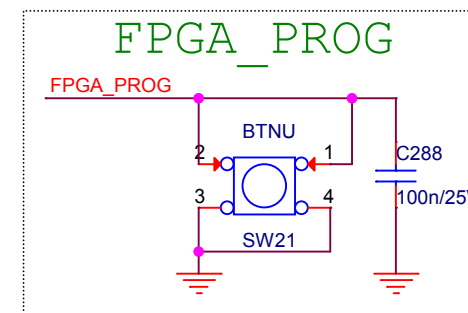
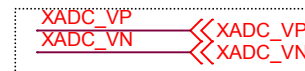
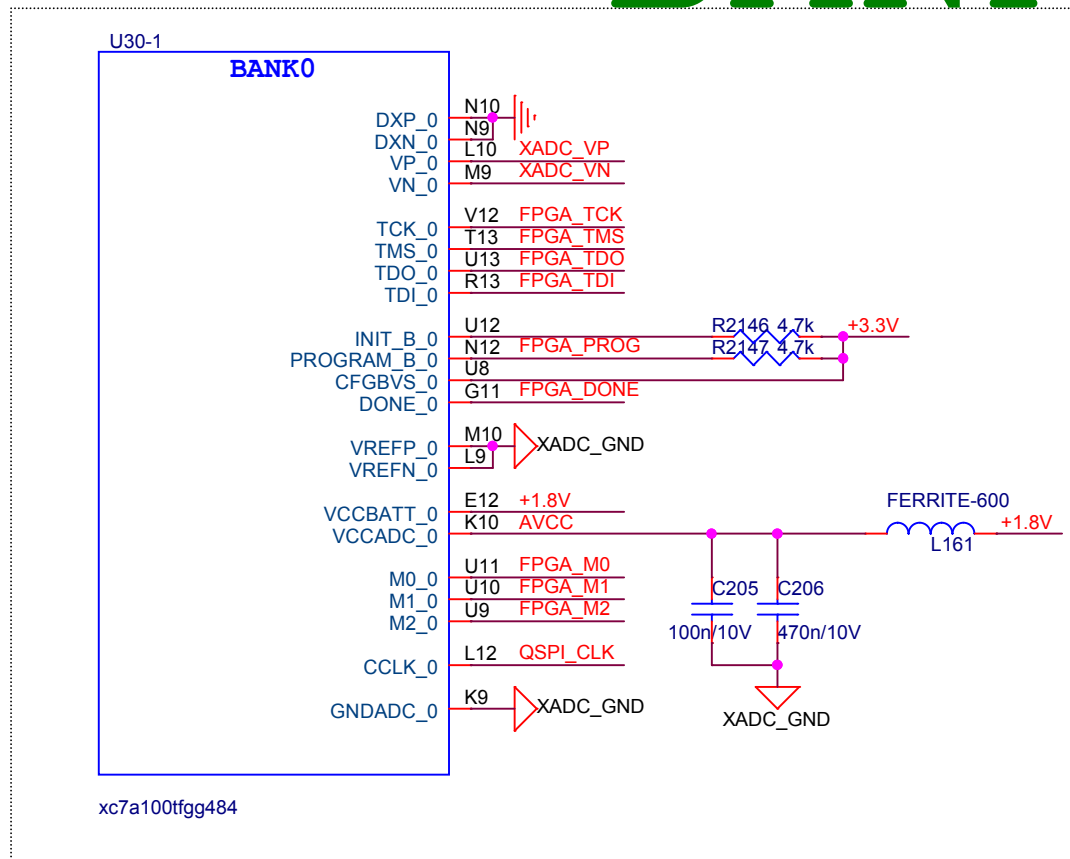
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E203 RISC-V评估板

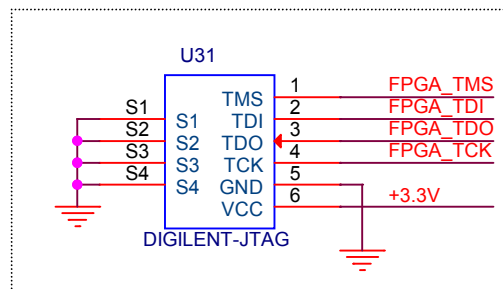
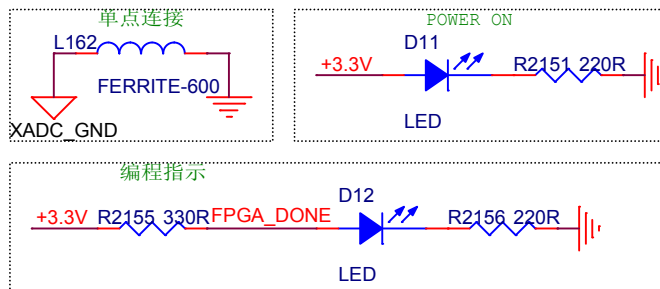
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BANK0



FPGA_JTAG



Title

E203 RISC-V评估板

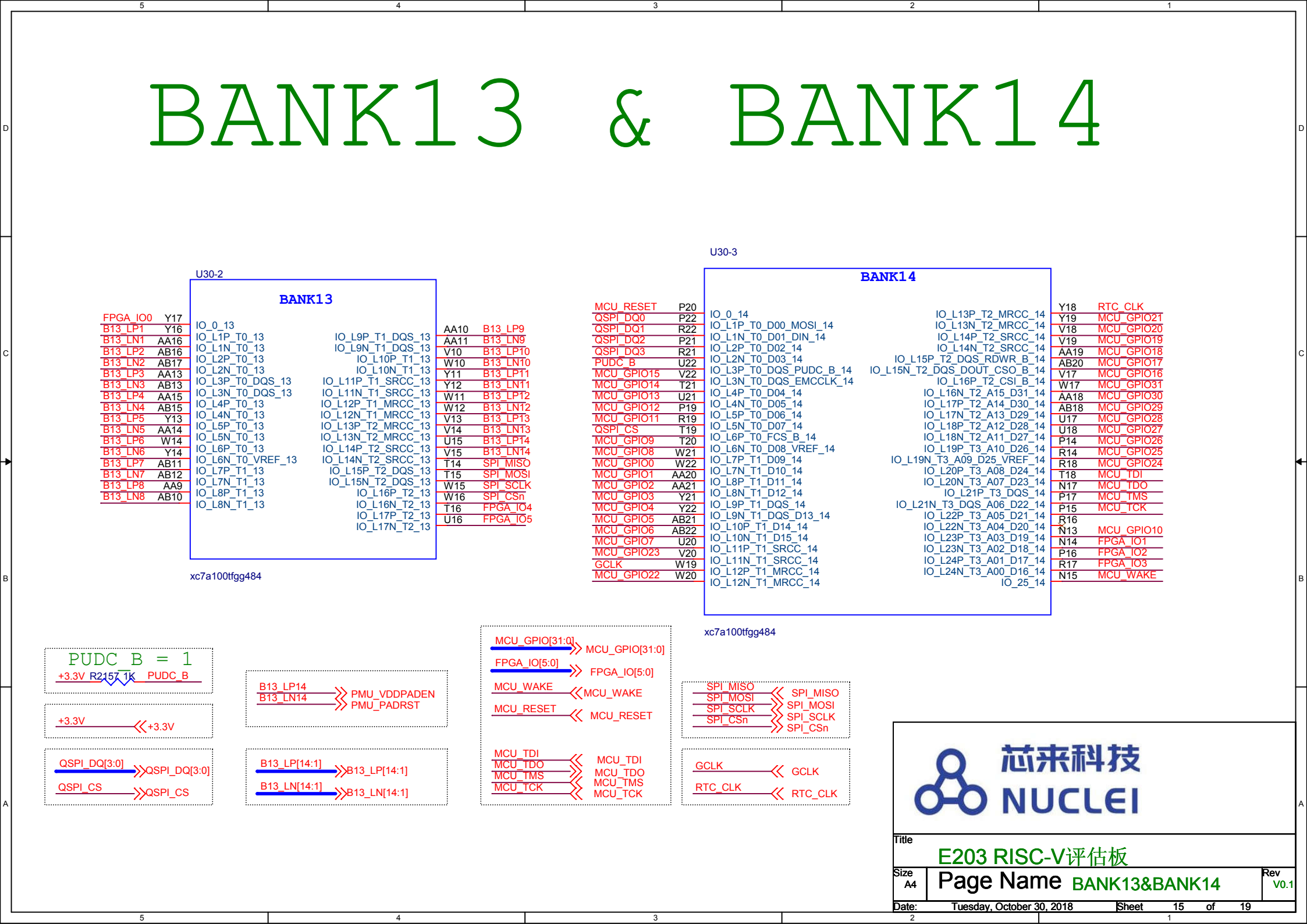
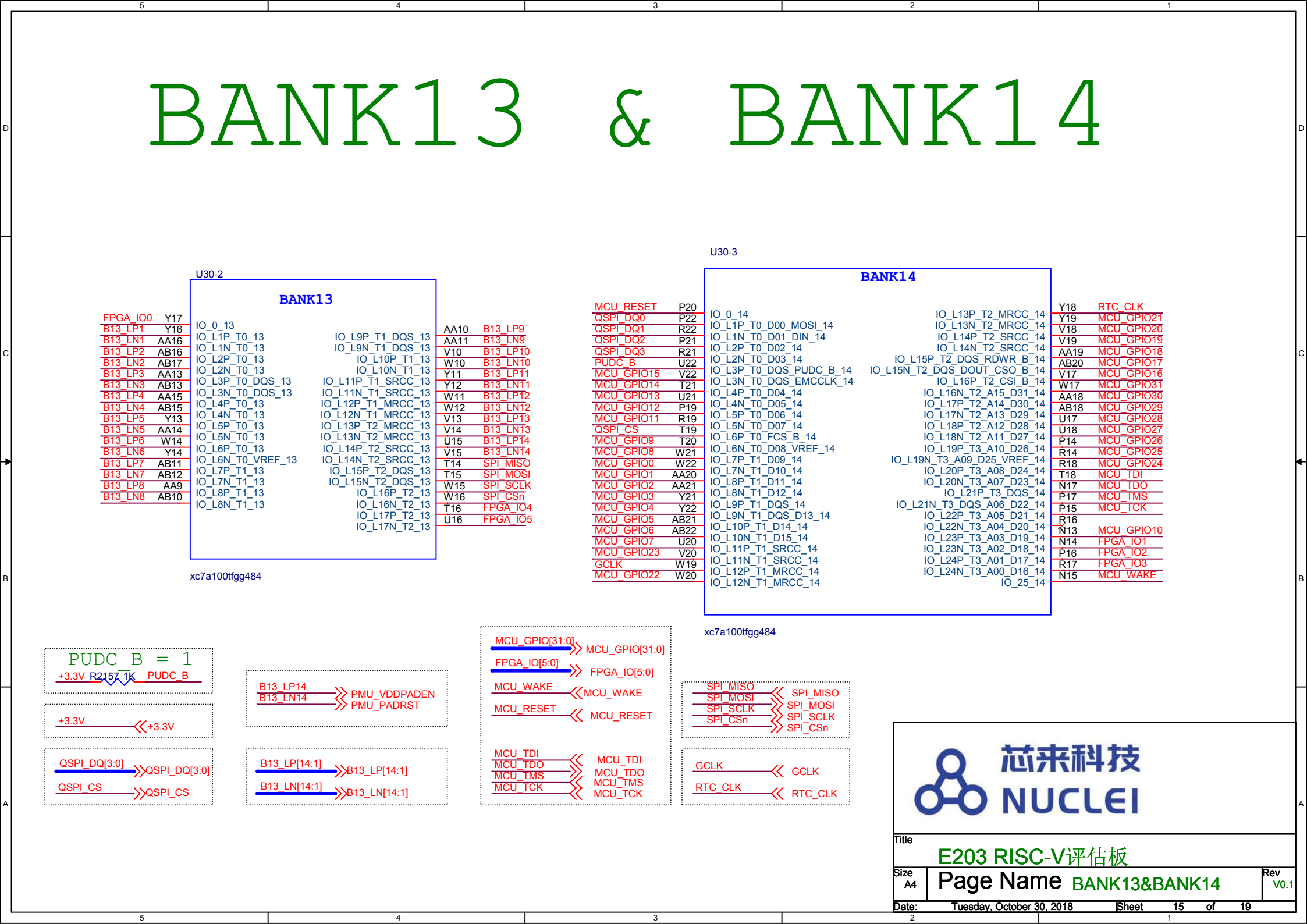
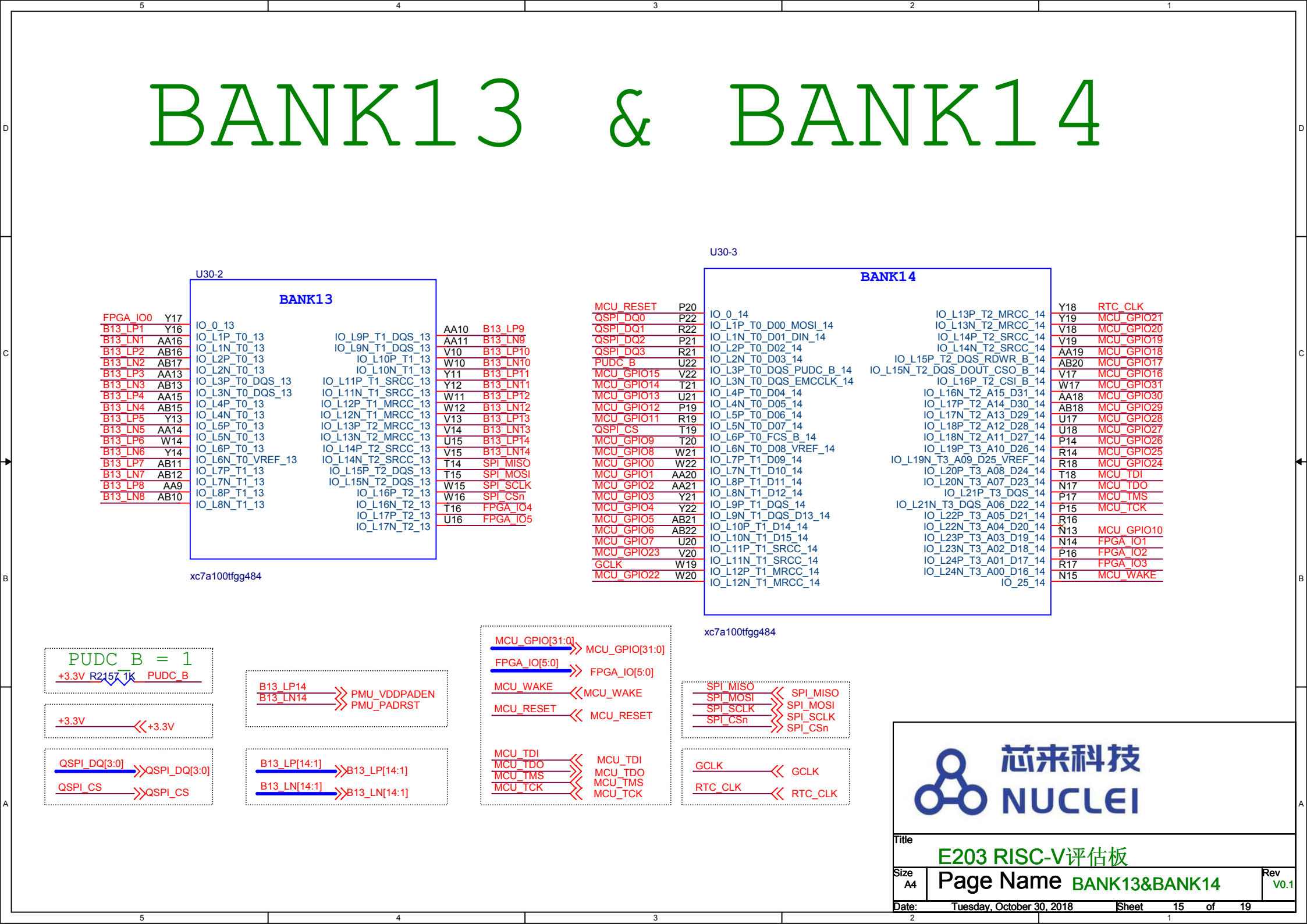
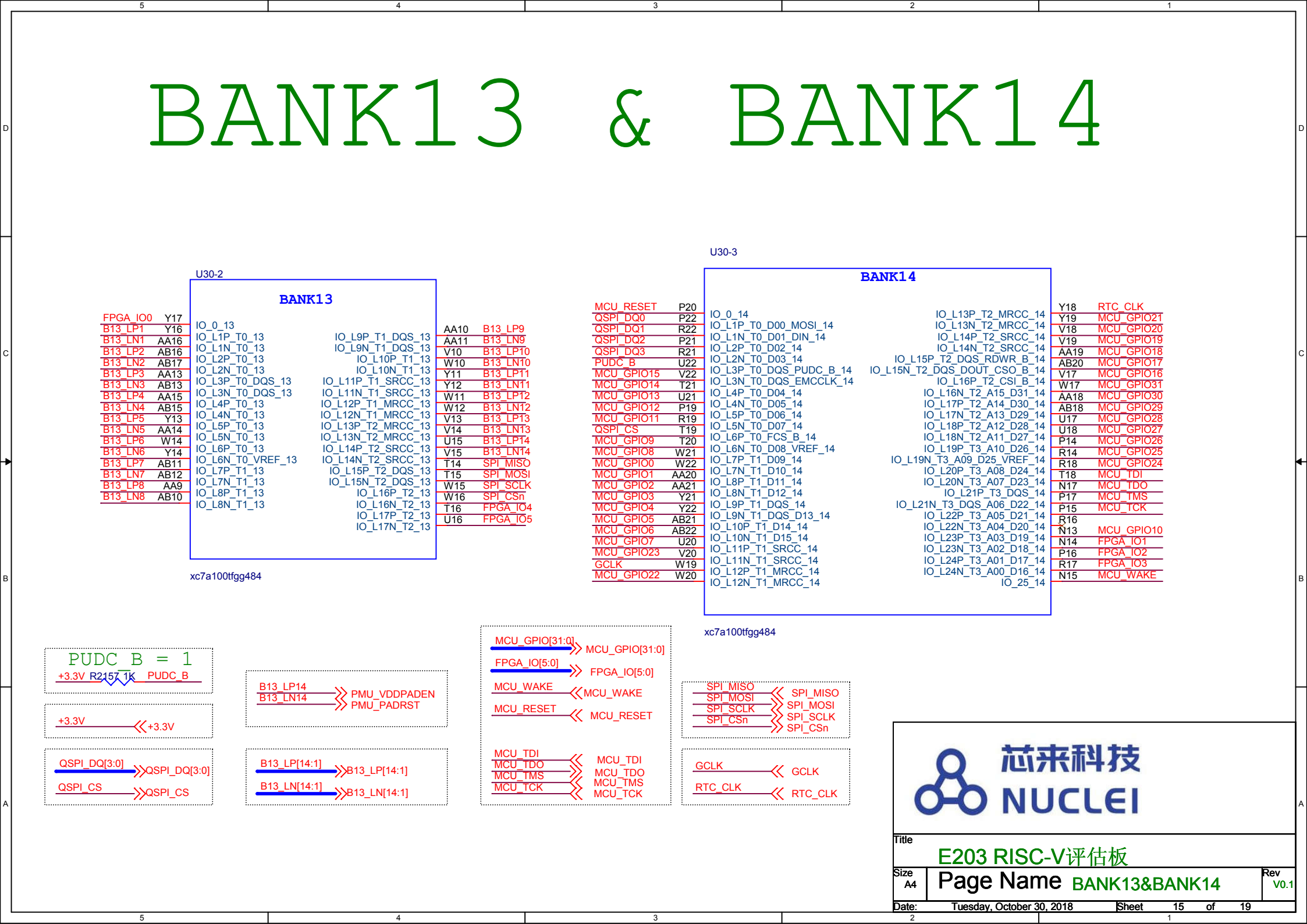
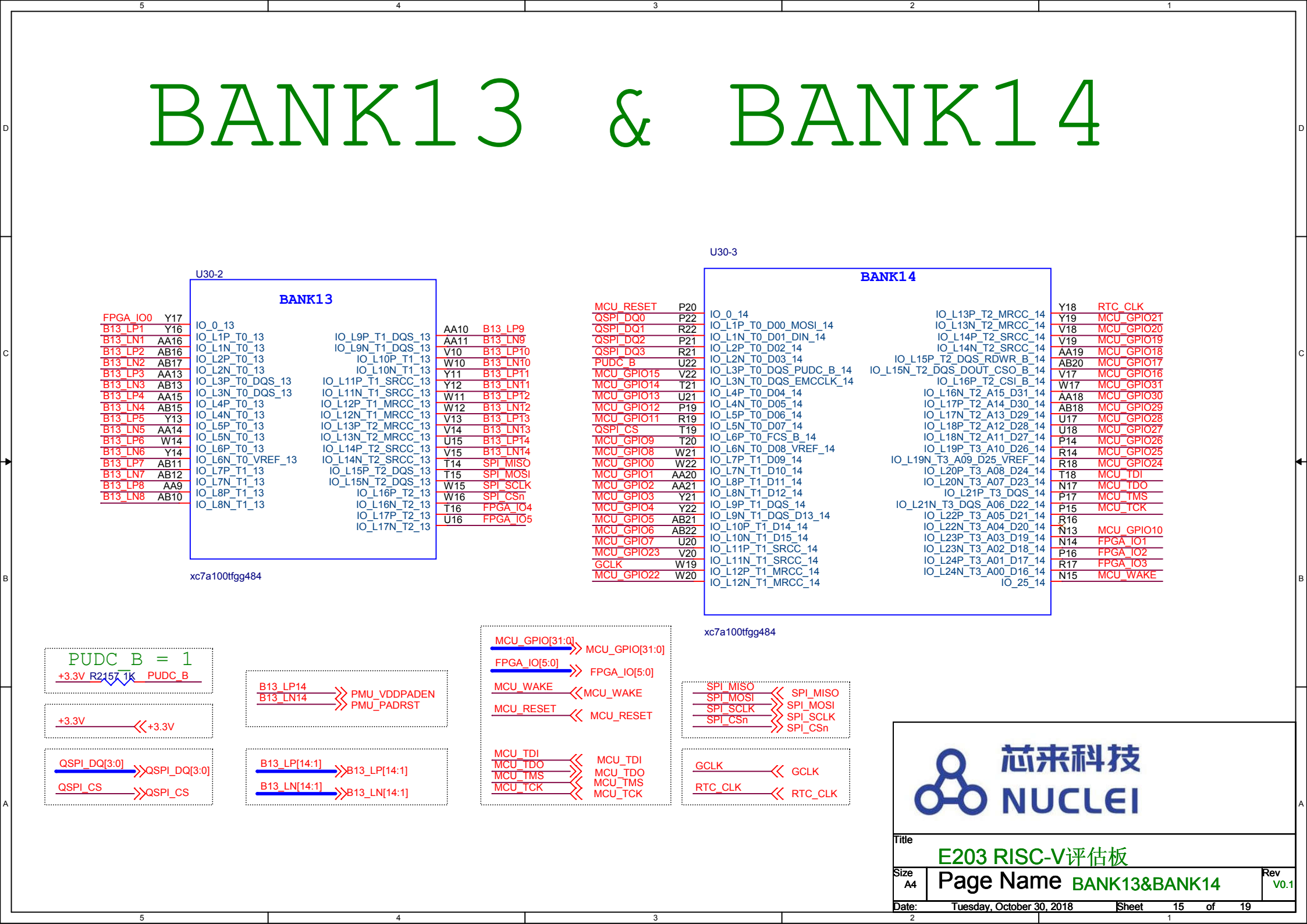
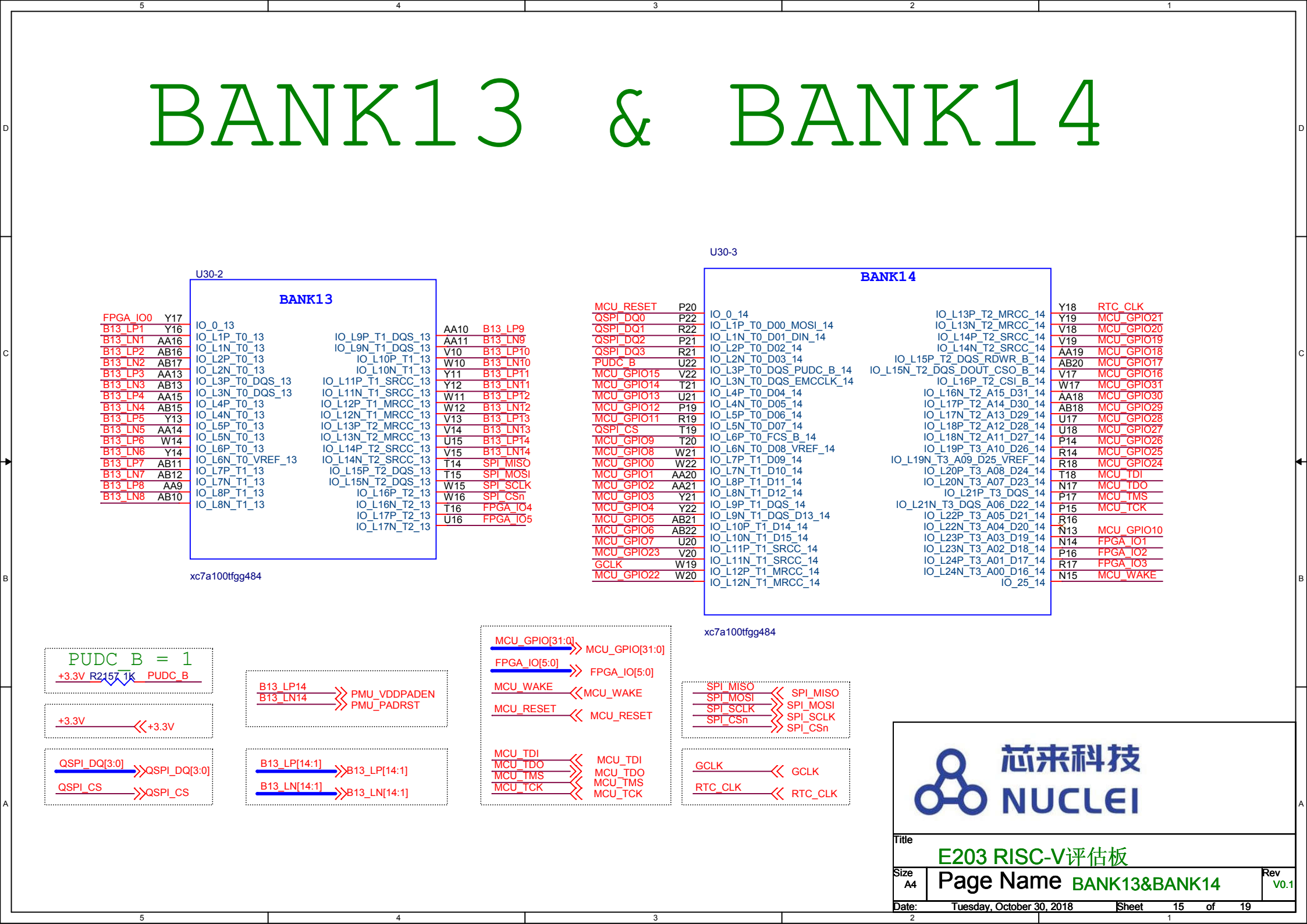
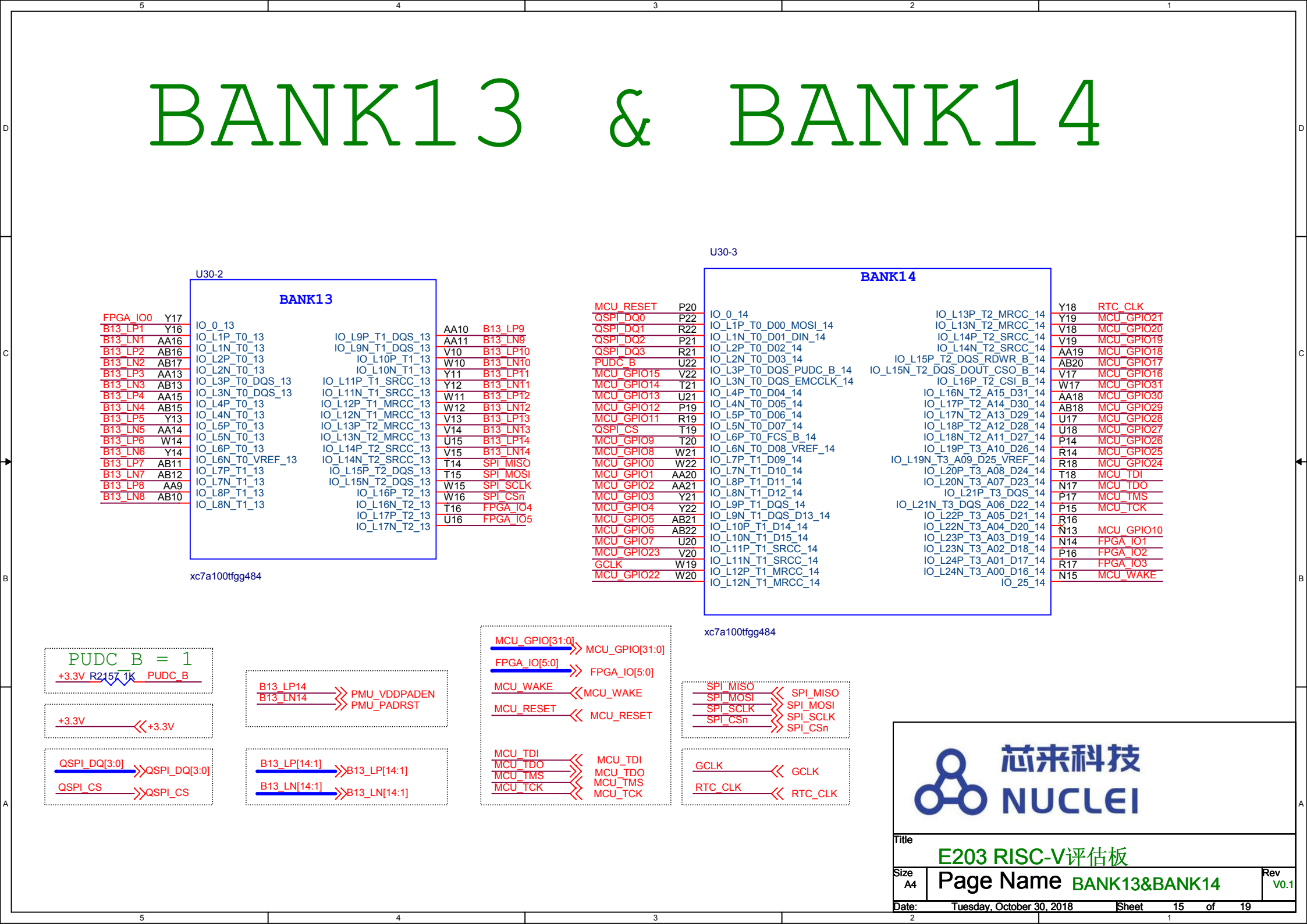
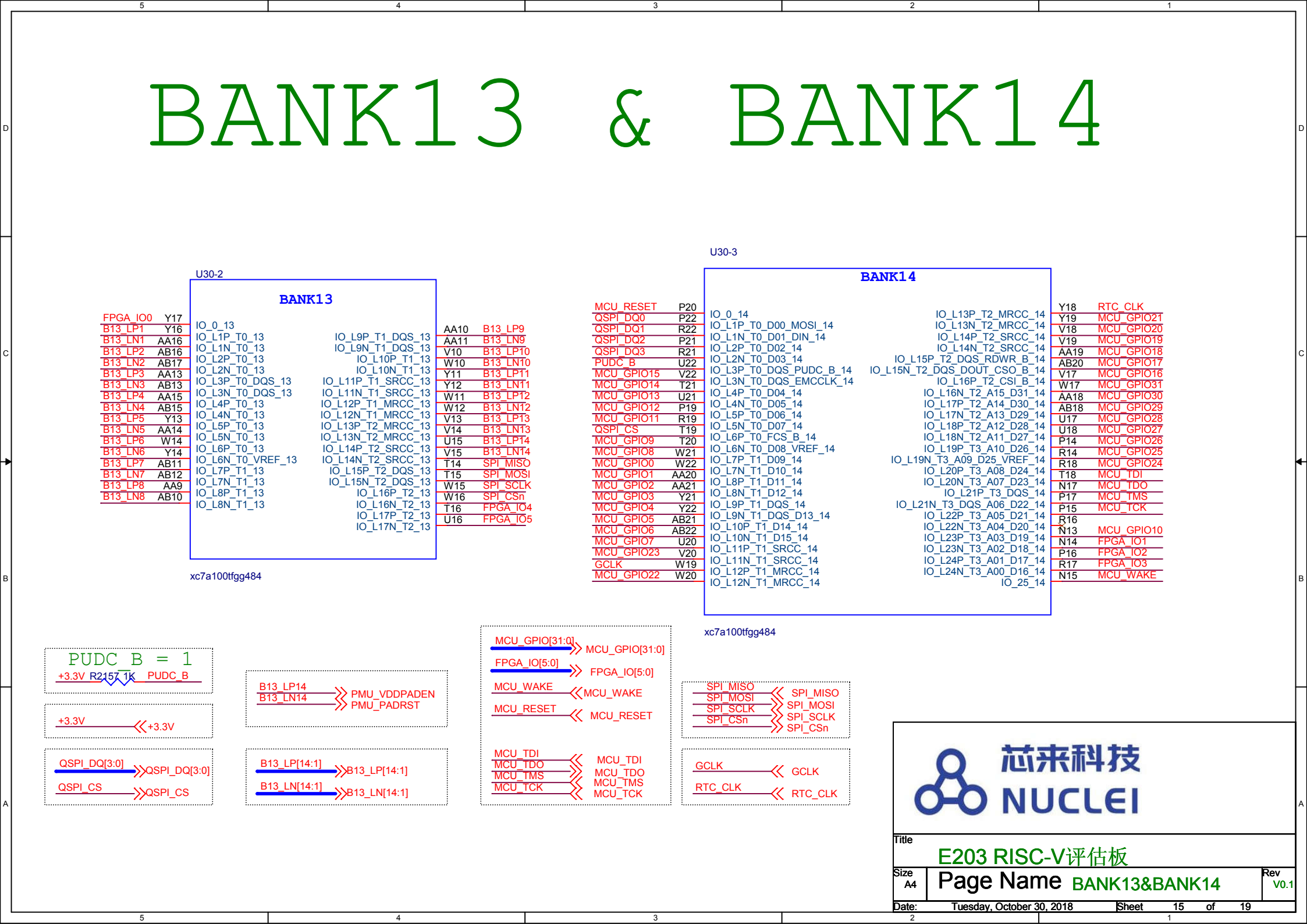
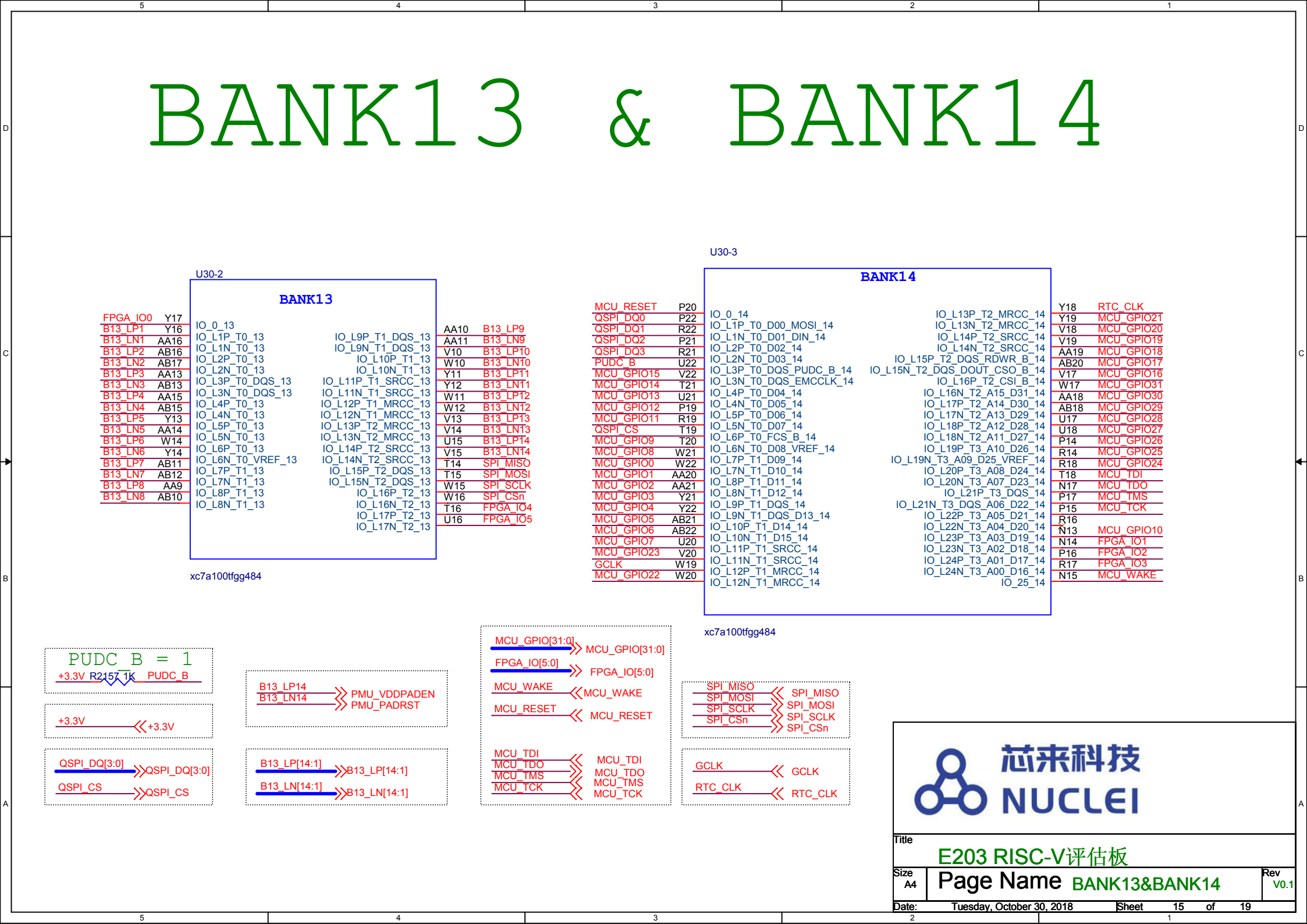
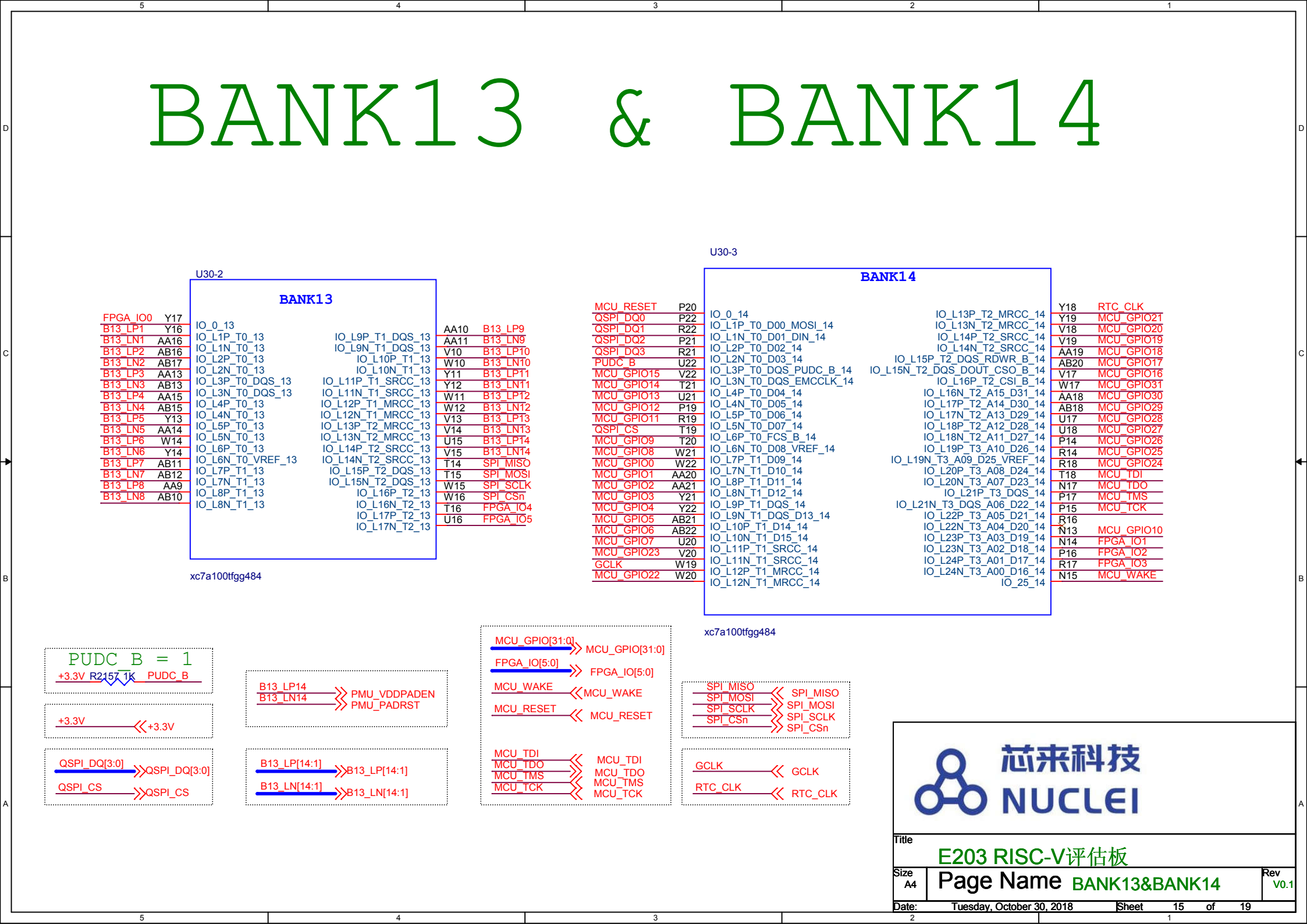
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BANK15 & BANK16

U30-4				BANK15			
B15_IO0	J16	IO_0_15		IO_L13P_T2_MRCC_15	K18	B15_LP13	
B15_LP1	H13	IO_L1P_T0_AD0P_15		IO_L13N_T2_MRCC_15	K19	B15_LN13	
B15_LN1	G13	IO_L1N_T0_AD0N_15		IO_L14P_T2_SRCC_15	L19	B15_LP14	
B15_LP2	G15	IO_L2P_T0_AD8P_15		IO_L14N_T2_SRCC_15	L20	B15_LN14	
B15_LN2	G16	IO_L2N_T0_AD8N_15		IO_L15P_T2_DQS_15	N22	B15_LP15	
B15_LP3	J14	IO_L3P_T0_DQS_AD1P_15	IO_L15N_T2_DQS_ADV_B_15	IO_L16P_T2_A28_15	M22	B15_LN15	
B15_LN3	H14	IO_L3N_T0_DQS_AD1N_15	IO_L16N_T2_A27_15	IO_L17P_T2_A26_15	M18	B15_LP16	
B15_LP4	G17	IO_L4P_T0_15	IO_L17N_T2_A25_15	IO_L18P_T2_A24_15	L18	B15_LN16	
B15_LN4	G18	IO_L4N_T0_15	IO_L18N_T2_A23_15	IO_L19P_T3_A22_15	N18	B15_LP17	
B15_LP5	J15	IO_L5P_T0_AD9P_15	IO_L19N_T3_A21_VREF_15	IO_L20P_T3_A20_15	N19	B15_LN17	
B15_LN5	H15	IO_L5N_T0_AD9N_15	IO_L20N_T3_A19_15	IO_L21P_T3_DQS_15	N20	B15_LP18	
B15_LP6	H17	IO_L6P_T0_15	IO_L21N_T3_DQS_A18_15	IO_L22P_T3_A17_15	M20	B15_LN18	
B15_LN6	H18	IO_L6N_T0_VREF_15	IO_L22N_T3_A16_15	IO_L23P_T3_FOE_B_15	K13	B15_LP19	
B15_LP7	J22	IO_L7P_T1_AD2P_15	IO_L23N_T3_FWE_B_15	IO_L24P_T3_RS1_15	K14	B15_LN19	
B15_LN7	H22	IO_L7N_T1_AD2N_15	IO_L24N_T3_RS0_15	IO_25_15	M13	B15_LP20	
B15_LP8	H20	IO_L8P_T1_AD10P_15			L13	B15_LN20	
B15_LN8	G20	IO_L8N_T1_AD10N_15			K17	B15_LP21	
B15_LP9	K21	IO_L9P_T1_DQS_AD3P_15			J17	B15_LN21	
B15_LN9	K22	IO_L9N_T1_DQS_AD3N_15			L14	B15_LP22	
B15_LP10	M21	IO_L10P_T1_AD11P_15			L15	B15_LN22	
B15_LN10	L21	IO_L10N_T1_AD11N_15			L16	B15_LP23	
B15_LP11	J20	IO_L11P_T1_SRCC_15			K16	B15_LN23	
B15_LN11	J21	IO_L11N_T1_SRCC_15			M15	B15_LP24	
B15_LP12	J19	IO_L12P_T1_MRCC_15			M16	B15_LN24	
B15_LN12	H19	IO_L12N_T1_MRCC_15			M17	B15_IO25	

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U30-5				BANK16			
B16_IO0	F15	IO_0_16		IO_L13P_T2_MRCC_16	C18	B16_LP13	
B16_LP1	F13	IO_L1P_T0_16		IO_L13N_T2_MRCC_16	C19	B16_LN13	
B16_LN1	F14	IO_L1N_T0_16		IO_L14P_T2_SRCC_16	E19	B16_LP14	
B16_LP2	F16	IO_L2P_T0_16		IO_L14N_T2_SRCC_16	D19	B16_LN14	
B16_LN2	E17	IO_L2N_T0_16		IO_L15P_T2_DQS_16	F18	B16_LP15	
B16_LP3	C14	IO_L3P_T0_DQS_16	IO_L15N_T2_DQS_16	IO_L16P_T2_16	E18	B16_LN15	
B16_LN3	C15	IO_L3N_T0_DQS_16	IO_L16N_T2_16	IO_L17P_T2_16	B20	B16_LP16	
B16_LP4	E13	IO_L4P_T0_16	IO_L17N_T2_16	IO_L18P_T2_16	A20	B16_LN16	
B16_LN4	E14	IO_L4N_T0_16	IO_L18N_T2_16	IO_L19P_T3_16	A18	B16_LP17	
B16_LP5	E16	IO_L5P_T0_16	IO_L19N_T3_VREF_16	IO_L20P_T3_16	A19	B16_LN17	
B16_LN5	D16	IO_L5N_T0_16	IO_L20N_T3_16	IO_L21P_T3_DQS_16	F19	B16_LP18	
B16_LP6	D14	IO_L6P_T0_16	IO_L21N_T3_DQS_16	IO_L22P_T3_16	F20	B16_LN18	
B16_LN6	D15	IO_L6N_T0_VREF_16	IO_L22N_T3_16	IO_L23P_T3_16	D20	B16_LP19	
B16_LP7	B15	IO_L7P_T1_16	IO_L23N_T3_16	IO_L24P_T3_16	C20	B16_LN19	
B16_LN7	B16	IO_L7N_T1_16	IO_L24N_T3_16	IO_25_16	C22	B16_LP20	
B16_LP8	C13	IO_L8P_T1_16			B22	B16_LN20	
B16_LN8	B13	IO_L8N_T1_16			B21	B16_LP21	
B16_LP9	A15	IO_L9P_T1_DQS_16			A21	B16_LN21	
B16_LN9	A16	IO_L9N_T1_DQS_16			E22	B16_LP22	
B16_LP10	A13	IO_L10P_T1_16			D22	B16_LN22	
B16_LN10	A14	IO_L10N_T1_16			E21	B16_LP23	
B16_LP11	B17	IO_L11P_T1_SRCC_16			D21	B16_LN23	
B16_LN11	B18	IO_L11N_T1_SRCC_16			G21	B16_LP24	
B16_LP12	D17	IO_L12P_T1_MRCC_16			G22	B16_LN24	
B16_LN12	C17	IO_L12N_T1_MRCC_16			F21	B16_IO25	

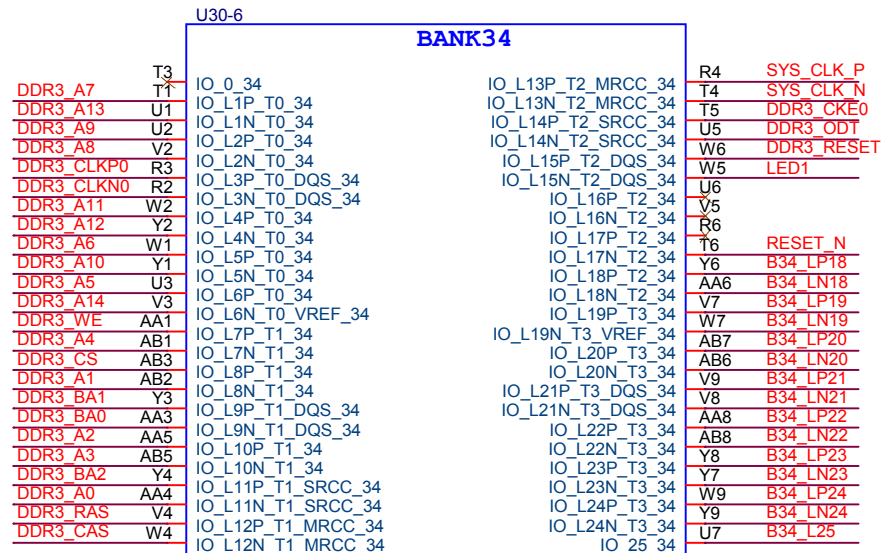
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B15_IO0 >>> B15_IO0
B15_IO25 >>> B15_IO25
B15_LP[24:1] >>> B15_LP[24:1]
B15_LN[24:1] >>> B15_LN[24:1]

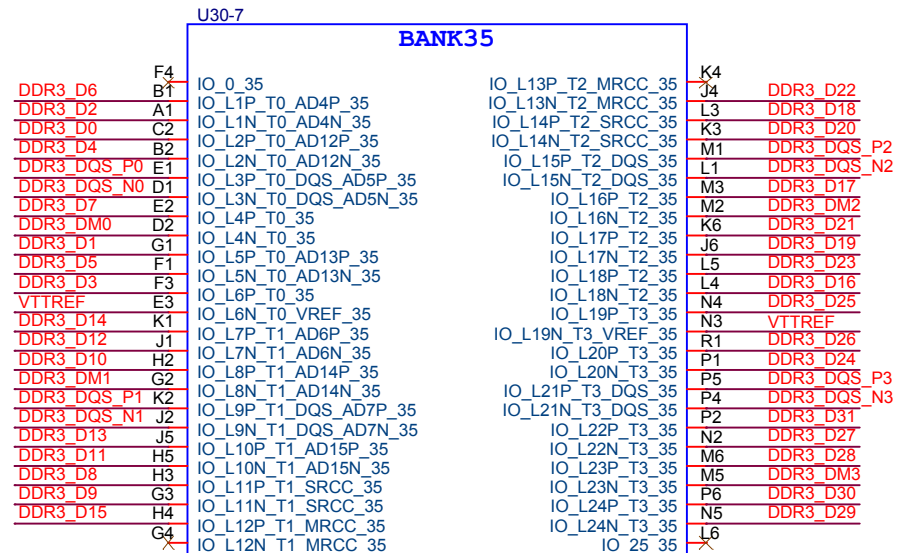
B16_IO0 >>> B16_IO0
B16_IO25 >>> B16_IO25
B16_LP[24:1] >>> B16_LP[24:1]
B16_LN[24:1] >>> B16_LN[24:1]



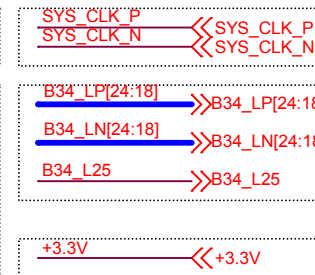
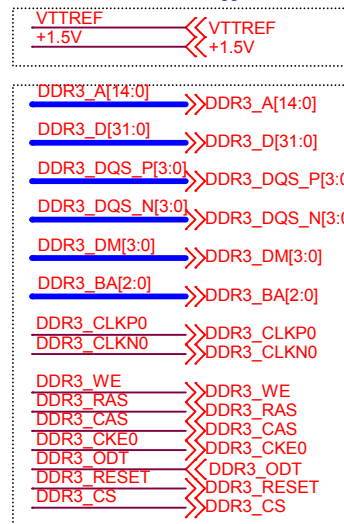
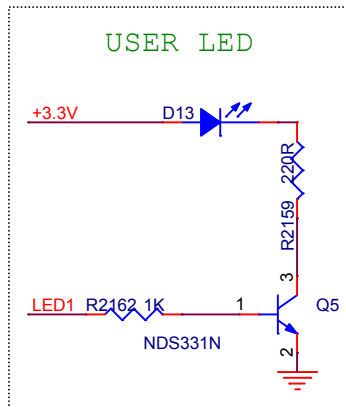
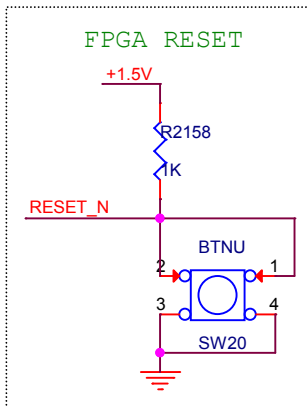
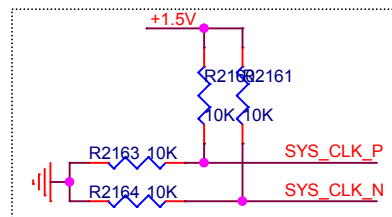
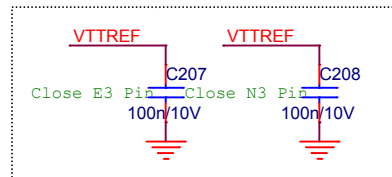
BANK34 & BANK35



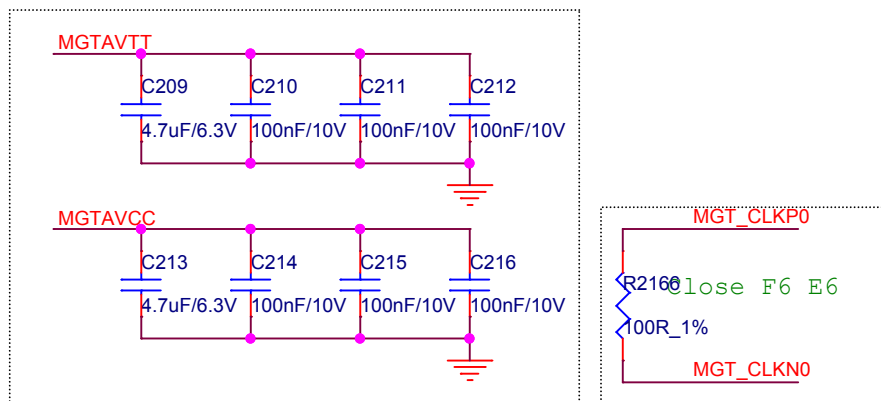
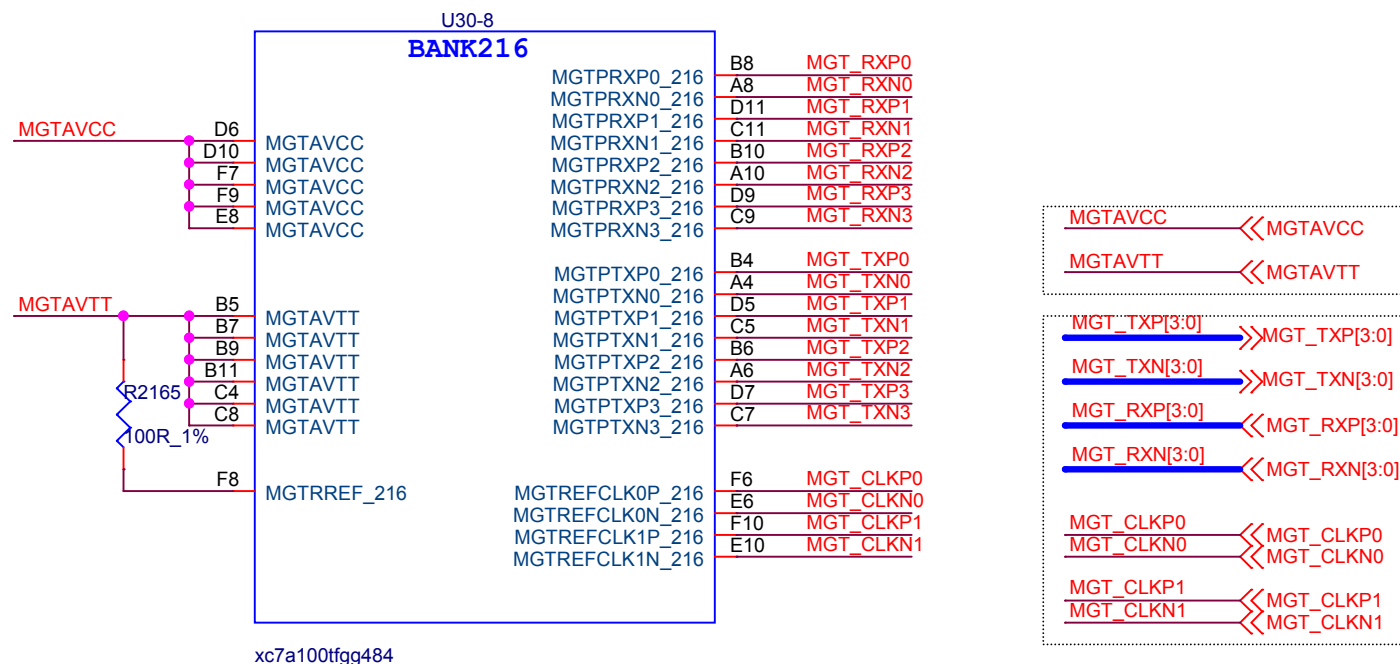
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BANK216



BANK POWER

